FABRICATION AND TESTING

OF HEATED ATOMIC FORCE MICROSCOPE CANTILEVERS

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By

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FABRICATION AND TESTING

OF HEATED ATOMIC FORCE MICROSCOPE CANTILEVERS

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SUMMARY

The invention of the atomic force microscope (AFM) revolutionized the scientific world by providing researchers with the ability to make topographical maps of both conducting and non-conducting surfaces with nanometer resolution. As an alternative to optical AFM methods, thermal cantilevers have been investigated as a method to measure topography. This study reports the fabrication and testing of heated AFM cantilevers.

This study transfers a fabrication process first developed at Stanford University to the Georgia Institute of Technology micro-fabrication facility and fabricates six different heated AFM cantilever designs. Selective impurity doping of a silicon cantilever allows it to become electrically conductive with a resistive element near the cantilever free end. Voltage applied across the cantilever legs induces current flow through the cantilever that generates heat in the resistive element.

A deep understanding of the operational behavior and limits of the AFM cantilever is required to use the cantilever as an experimental tool. Characterization experiments determined the cantilever electrical resistance and temperature response. Experiments were conducted that electrically test heated AFM cantilevers at various system input voltages. Electrical and thermal responses of these cantilevers were compared against a theoretical model. The model utilizes heat transfer fundamentals and links the thermal response to the cantilever temperature-dependent electrical characteristics. Results of this study show that the fabricated heated AFM cantilevers have a tip with a radius of curvature as small as 20nm. Cantilever

temperatures can exceed 700°C in short pulses and, because the resistive heating element is also a temperature sensor, calibration of the cantilever temperature response is possible to within 1°C.

CHAPTER I

INTRODUCTION

In 1986 the atomic force microscope (AFM) revolutionized the scientific world by providing researchers with the ability to make topographical maps of conducting and non-conducting surfaces with nanometer resolution [1]. This measurement system is very robust but there are limitations, particularly imaging speed. One way to improve speed would be to operate many cantilevers in parallel but optical detection of cantilever displacement does not easily accommodate an array of cantilevers for simultaneous imaging. Thus, other measurement systems that do not use laser deflection have been developed. Piezioresistive elements have been integrated into cantilevers to measure the strain induced in the cantilever as it flexes when following the contours of a surface [2]. More recently, heated AFM cantilevers have been investigated as another possible method for topography detection [3].

In an advanced data storage system developed at IBM Research it has been demonstrated that a heated AFM cantilever can be used to write indentations as small as 23nm in diameter into a polymer [4], as well as read back these indentations. The silicon cantilevers developed were made electrically active by selectively implanting different quantities of impurities into the legs and the tip platform of each cantilever. Selective implantation produced a cantilever with highly conductive legs and a resistive region near the tip, as shown in Figure 1. By applying a voltage across the legs of the cantilever, the

current generated produces heat in the resistive tip region which is carried to the legs via thermal conduction.

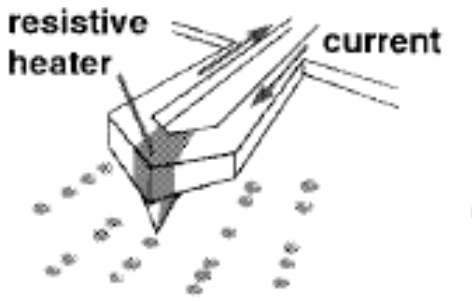


Figure 1. Heated AFM cantilever [3].

The electrical resistance of the cantilever is a function of temperature, thus to measure its resistance a thermally stable resistive element is needed in series with the cantilever. To aid in the cantilever resistance measurement and to maximize sensitivity, a sense resistor is added in series with the heated AFM cantilever, as shown in Figure 2.

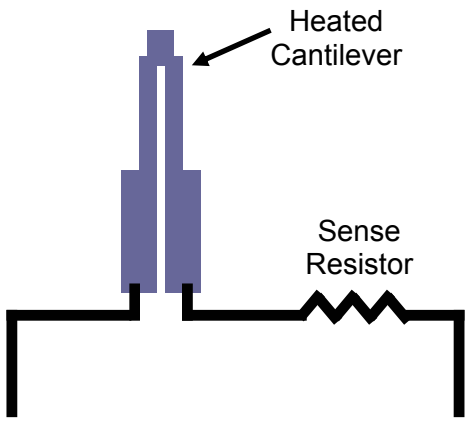


Figure 2. Electrical circuit used with heated AFM cantilevers.

The resistive heating of the cantilever free end gives the device the ability to write on a substrate. By heating the tip above the glass transition temperature of the substrate polymer melting takes place, as in Figure 3.

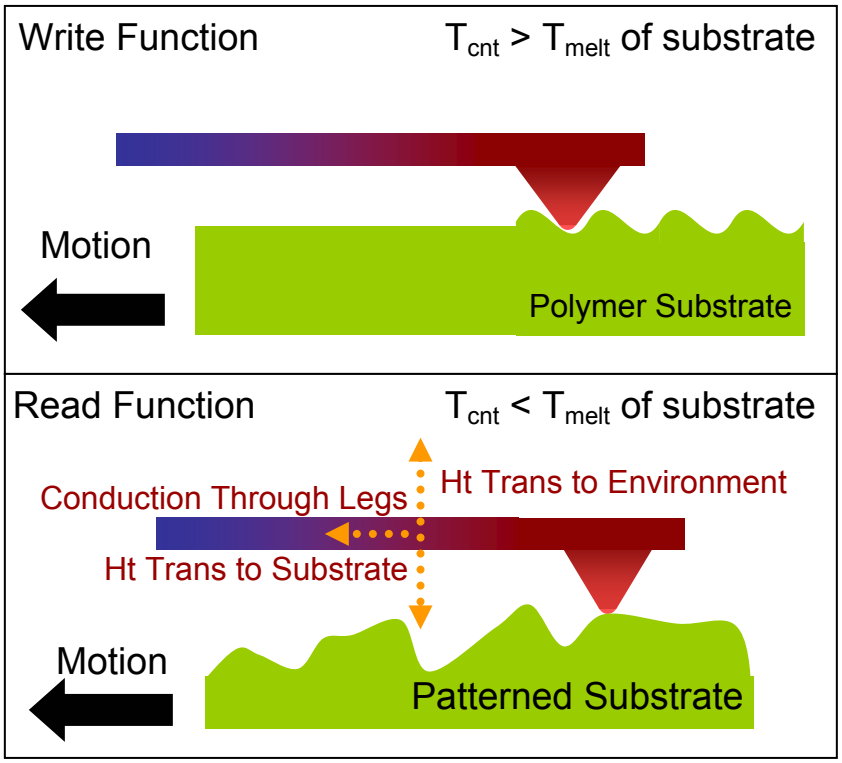


Figure 3. Thermal writing and reading with a heated AFM cantilever.

The reading/imaging function of a heated AFM cantilever uses thermal interactions between the cantilever and the imaging surface, rather than optical methods, to image the surface. As the cantilever traverses the contours of a surface the distance separating the cantilever legs and surface will increase or decrease. A variation in this distance influences the heat transfer between the cantilever legs and the imaging surface and heats or cools the cantilever accordingly. These changes in temperature produce

changes in the cantilever resistance and by monitoring the resistance the surface is imaged. Figure 3 illustrates this function.

A voltage applied across the sense resistor and the cantilever, typically in the 1 to 10V range, generates heat in the cantilever free end. Care must be taken such that the applied voltage does not heat the tip temperature higher than the melting point of the imaging surface as the tip can melt the surface features. However the data storage writing function requires surface melting. As the cantilever traverses the surface contours, changes in the thermal interaction between the two surfaces generate temperature changes in the cantilever legs. Changes in cantilever temperature induce changes in the measured cantilever resistance which is monitored across the sense resistor and converted into a corresponding topographic image.

Heated AFM cantilevers show the potential to have superior resolution and be better suited for use in array applications than current AFM and piezoresistive technologies [5]. This self-contained system has the potential for size and space reduction compared to other systems that have already reached their minimum size limitations. By building arrays of cantilevers, parallel imaging, force measurement, or nanolithography can be preformed.

This thesis describes fabricating and characterizing heated AFM cantilevers. The project design and development requires a highly integrated approach that couples heat transfer analysis, mechanical and electrical design, and micro-fabrication. Modeling and experimental measurements determine the interactions and limitations of modifying the overall size and shape of the beam, while fabrication limitations will play a large role in determining the resulting feature sizes.

CHAPTER II

BACKGROUND AND LITERATURE REVIEW

In almost every field of scientific study researchers need the ability to image surfaces down to sub-nanometer scales, but it was not until recently that this capability existed. There are many different ways that a surface or feature can be measured; optically, using the electrical properties of the surface, or physically touching the surface with a device. Optical microscopy is restricted by the diffraction limits of visible light, and therefore limits the resolution of structures that are significantly smaller than the 300 - 700 nm wavelength of visible light. A scanning electron microscope (SEM) uses the electrical properties of a sample to provide nanometer resolution. SEM is effective only for conductive samples and provides only two-dimensional information. Imaging a surface using physical methods, such as profilometry or AFM have proven to provide sub-nanometer resolution and can be conducted on many different surfaces, whether conductive or not.

2.1 Atomic Force Microscopy (AFM)

The most widely used nano-scale imaging technique is to bounce a laser beam off the backside of an AFM cantilever and onto a position sensitive detector (PSD). The PSD is a segmented photodiode that detects position by taking the difference between the amounts of light impinging on the upper and lower segments of the diode. As the cantilever traverses a surface and is deflected, the reflect laser beam angle changes with respect to the vertical axis. This angle change causes the laser spot to shift on the PSD

thus changing the voltage difference between the upper and lower segments. This method is detailed in Figure 4. The power of the optical lever lies in the fact that because it is the reflected angle that changes when the cantilever deflects, the farther away the PSD is from the cantilever, the more magnified the laser spot translation will be with respect to the cantilever deflection. This allows for extremely high potential resolution in the vertical direction [1].

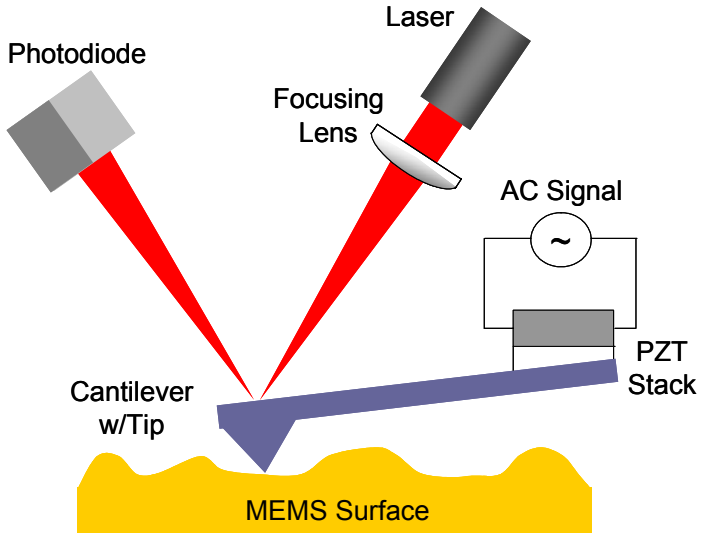


Figure 4. Diagram of an atomic force microscope system.

The PSD-limited resolution of an optical lever AFM is near 10^{-4} angstroms, which yields ample resolution for imaging purposes. In practice, however, the resolution is limited by the amplitude of the thermal vibration of the cantilever, which is generally less than an angstrom at room temperature [6].

There are many advantages of the optical lever measurement technique for cantilever deflection, the largest being ease of use. Alignment of the laser onto the backside of the cantilever is only necessary in two dimensions, which can be easily done

with an optical microscope. Once aligned to the cantilever, the reflected laser signal must be aligned to the PSD, which is done through the use of an adjustable mirror and a translatable PSD. Further adding to the simplicity, the voltage output of the PSD is simply correlated to the true cantilever deflection.

The AFM does have some drawbacks, the most significant being the optical interference artifact. This drawback introduces regularly spaced wavy lanes across an image [7]. Another drawback is the need for external hardware, as opposed to the internal electronics used for measuring cantilever deflection with piezoresistive and thermal techniques. The necessary external equipment may be inconvenient in potentially portable applications using AFM technology where compactness may be significant [4].

2.2 Other Cantilever Deflection Measurement Methods

Early in the development of AFM, other functional deflection detection methods existed but were quickly replaced by more-effective techniques. This section gives a basic outline of these techniques.

2.2.1 Scanning Tunneling Microscope (STM)

In STM, a sharp tungsten tip is brought into close proximity of a surface, and a bias is applied between the two. The applied voltage induces an electron tunneling current between the tip and the surface [8]. The tunneling current exhibits an exponential dependence on the tip-sample separation; therefore as the sample is translated beneath the tip the tunneling current changes due to variations in the sample height. In imaging applications the sample is moved laterally beneath the tip while the tunneling current is kept constant. Feedback from the tunneling current and a piezo actuator adjust the

sample height to compensate for variations in surface topography. By tracking the vertical actuation, which directly corresponds to the surface topography, a surface image is generated.

The tunneling current used in STM only occurs between two conductors; hence STM can only measure the height of conducting surfaces. To overcome this limitation, the backside of a micromachined cantilever with a sharp tip was covered in metal and used to trace the surface being imaged. The tunneling current was reflected off the back side of the cantilever thus using the cantilever deflection as a way to measure the topography of non-conducting surfaces.

The vertical resolution obtainable with STM is as low as 10^{-5} nm, but the difficulties inherent in its use are significant. Aligning the STM tip to the cantilever is very difficult, and contamination on the back of the cantilever or STM tip can have drastic effects on the sensitivity of the tunneling current [9]. Roughness on the back of the cantilever can also affect the tunneling current. Furthermore, in applications where the AFM cantilever is excited at its resonance frequency the STM loses its effectiveness because the tunneling gap becomes too large [10]. For these reasons, using STM to measure cantilever deflection was quickly abandoned in favor of optical methods.

2.2.2 Optical Interferometry

Optical interferometry is similar to AFM methods in that a laser, photodiode and cantilever are used simultaneously to record a surface's topography. But with optical interferometry the laser beam is split into two. Part of the signal is directed towards the photodiode and the rest is focused onto the backside of a micromachined cantilever. The cantilever reflects the laser to the photodiode, where it interferes with the part of the

beam that was split directly to the photodiode. As the cantilever deflects the interference pattern between the two incident beams also changes. Changes in the interference pattern vary the amount of light sensed by the photodiode and can be used in the feedback loop to maintain a constant cantilever deflection.

Optical interferometry offers several advantages and equally high resolution over STM deflection measurement. Advantages included ease of implementation, reliability, and less sensitivity to cantilever roughness [10]. The use of optical interferometry was brief due to the development of the AFM system, which improved upon the interferometry system and quickly surpassed it.

2.2.3 Piezoresistive Detection

Shortly after the initial invention of the AFM, imaging using a piezoresistive cantilever to measure deflection was developed as a way to integrate the deflection sensing instrumentation directly into the cantilever itself. In piezoresistive AFM, as forces are exerted on the AFM tip, an internal piezoresistive element senses the stresses induced by the tip deflection. Internal stresses lead to changes in the piezoresistive element resistance, which is measured using a Wheatstone bridge circuit and output as a voltage. With signal amplification and calibration, the voltage can be correlated to a known deflection of the cantilever.

Applying stress to a piezoresistor induces a change in resistivity which can be translated into a measurable change in resistance. Silicon, when doped, strongly exhibits piezoresistivity. For example, a boron doped cantilever surface with a nominal resistance of several kΩ exhibits a resistance change of a few percent when deflected 1 μm, making doped silicon very sensitive to small deflections [2]. Considering that micro-fabrication

techniques for silicon are already well established, silicon makes an excellent material choice for the fabrication of piezoresistive beams.

Piezoresistive cantilever resolution is limited by typical electrical noise sources, including amplifier noise, Johnson noise (frequency independent noise due to thermal energy in the resistor), and 1/f noise (due to conductance fluctuations at lower frequencies). Amplifier noise can be reduced by increasing the bias voltage on the bridge circuit that detects the piezoresistive resistance change, but doing so also leads to increases in temperature of the piezoresistive element, which can cause changes in resistivity. Little can be done to avoid Johnson noise aside from operating at low temperatures or reducing the resistance, which for many applications is not feasible. Reduction in the 1/f noise can be achieved by increasing the concentration of free electrons in the piezoresistor, however doing so also decreases the degree of piezoresistivity, decreasing the sensitivity [11]. In practice, piezoresistive cantilevers can resolve vertical features below 1nm and in many cases can resolve sub-atomic distances, depending on the piezoresistive sensitivity and the electronics used.

The largest advantage for piezoresistive cantilever beams when compared to other methods is the integration of the deflection-sensing instrumentation onto the cantilever. This minimizes the amount of physical space required for the AFM, allowing the AFM to be easily incorporated into a vacuum or low temperature system.

The primary disadvantage of piezoresistive detection is the piezoresistor sensitivity due to changes in temperature. Through thermal cycling, the implanted impurities can be driven deeper into the cantilever which changes the resistance and

overall sensitivity of the cantilever. During use, distortions could occur when imaging surfaces with temperature gradients.

2.2.4 Thermal Imaging

In the process of developing an alternative data storage form based on AFM technology, researchers at IBM Zurich developed a cantilever deflection measurement technique known as thermal imaging [4]. A computer generated image of data taken with a thermal cantilever is shown in Figure 5.

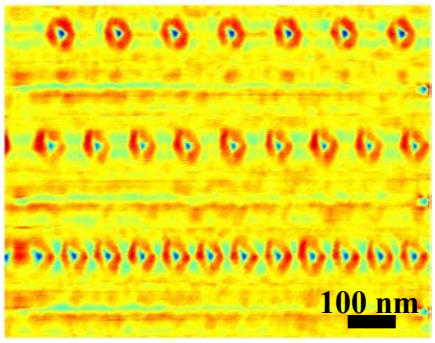


Figure 5. Thermal image of pits indented into a polymer. Pits made with heated AFM cantilever [12].

Thermal conduction between the cantilever and the substrate governs cantilever sensitivity. There are upper and lower limits to the conduction between these two surfaces, and these limits impact the design of the tip height. A tip height that is too tall removes any conduction between the legs and the substrate thereby eliminating the thermal sensitivity. A tip that is too short, within several mean free path lengths of air, decreases the conduction between the two surfaces which decreases the thermal sensitivity. At such short length scales conduction becomes ballistic. In general, the

most sensitive cantilevers for imaging are those with short tips and thin cross sections [12].

To further increase the sensitivity of the cantilever, a thermal constriction was added to the cantilever design. This restriction is a reduction in width of the cantilever between the legs and the heater, as shown in Figure 6 . By reducing the cantilever width the ability for heat to pass from the tip through the legs decreases. This has been shown to increase the sensitivity [12]. Thermal cantilever sensitivity has been shown to yield a vertical resolution as good as AFM techniques, and better than that of piezoresistive cantilevers.

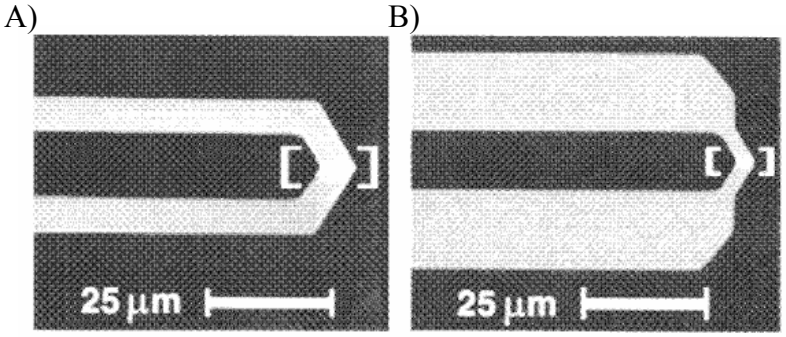


Figure 6. A) Non-constricted cantilever. B) Constricted cantilever. [3]

Like piezoresistive cantilevers, the biggest advantage of the thermal cantilevers is the integration of the sensing device directly into the cantilever itself. The integration carries with it the same advantages as those for piezoresistive detection in terms of space requirements, vacuum or other controlled environment integration, and cantilever array possibilities. Thermal cantilevers also offer improved imaging resolution over piezoresistive cantilevers.

The biggest disadvantage of thermal cantilevers is the novelty of the technique. The techniques described previously have been used for many years and are well understood and characterized. Thermal imaging is still in its infancy stage and the amount of information and practical experience available is limited.

Similar to piezoresistive cantilevers, thermal cycling can cause dopant diffusion, in this case from the heater region to the cantilever legs. This only becomes an issue at high temperatures.

CHAPTER III

DESIGN & FABRICATION OF HEATED CANTILEVERS

This chapter focuses on the heated AFM cantilever design and fabrication details. Much of the design and fabrication steps were adapted from the research done by the Stanford [3] and IBM Zurich Research Laboratory groups [13], but modified to fit the Georgia Institute of Technology Microelectronics Research fabrication facility. In the subsequent sections cantilever physical design details are given followed by a comprehensive description of the fabrication process.

3.1 Heated AFM Cantilever Design

The cantilevers made and used in this study, although visually simple, are complex in their design and fabrication. To aid in the design benchmarks, geometries, and dimensions that were previously established were adopted. The geometry and benchmark template greatly increased the chances of successfully designing and fabricating a heated AFM cantilever.

3.1.1 Heated AFM Cantilever Benchmarks

The ideal heated AFM cantilever needs to satisfy many conditions in order to be competitive with traditional AFM surface imaging techniques. Heated AFM cantilevers must have a tip with a radius of curvature at or below 500Å, be capable of detecting 10Å of motion within the reading bandwidth, and have the highest possible natural frequency. To avoid wear of the tip and/or the imaging surface the cantilever needs to be soft at 1N/m or less. Finally, for efficiency during imaging the thermal time constant must be as

short as possible, on the order of 1μs or less [3]. These key parameters, spring constant, natural frequency, and cantilever electrical resistance were the focus when designing the heated AFM cantilevers.

3.1.1.1 Spring Constant

The spring constant, k, of the cantilever is a measure of mechanical compliance to an applied force. A cantilever that is too soft limits the force applied to the surface during imaging, while a cantilever that is too stiff damages itself or the surface being imaged. The cantilever spring constant, equation (3.1), is a function of force ,F, and deflection, δ.

$$k = \frac{F}{\delta} = \frac{F}{FL^3 \diagup 3EI} = \frac{EWt^3}{4L^3} \tag{3.1}$$

Deflection, though, is a function of force and by combining these quantities in the spring constant equation the force dependence is removed. The resulting equation leaves spring constant as only a function of the cantilever geometry and Young's modulus, E (150 GPa). Where W is the cantilever width, and t is the cantilever thickness and L is cantilever length.

3.1.1.2 Natural Frequency

The natural frequency, ω_o, of the cantilever is directly related to the mass and spring constant of the cantilever by equation (3.2). For signal processing it is important that the natural frequency of the cantilever be as high as possible. To do this a compromise is necessary between a large spring constant and low mass.

An effective mass is used in place of the actual cantilever mass and represents the notion that only a portion of the cantilever is in motion during vibration rather than the

entire cantilever. Equation (3.3) calculates the effective mass by multiplying the cantilever mass by 0.24 [14].

$$\omega_o = \left(\frac{k}{m_{eff}} \right)^{1/2} \tag{3.2}$$

$$m_{effective} = 0.24 m_{cantilever} \tag{3.3}$$

3.1.1.3 Cantilever Electrical Resistance

For this study, two heater sizes were created, one slightly large in area than the other, but both with the same heater resistance. Cantilevers A-C have a heater platform 5μm by 10μm in size, and cantilevers D-E have a platform that is 8μm by 16μm in size. Using these dimensions, an assumed cantilever thickness of 1μm, a resistivity of 1e17 phosphorous atoms/cm^3, and equation (3.4) the resulting heater resistances for all cantilevers was estimated to be ~ 2800Ω. In equation (3.4) R is the resistance, ρ is the resistivity, L is the length, and A is the cross sectional area.

$$R = \rho \frac{L}{A} \tag{3.4}$$

3.1.2 Heated AFM Cantilever Design - Anchor & Thermal Restrictions

Cantilevers fabricated by IBM Zurich had two unique features: an anchor that attached the cantilever to the base silicon substrate and a thermal restriction between the legs and heater platform. Each physical feature provided a specific fabrication and/or application advantage. Figure 7 shows the constituents of a heated AFM cantilever.

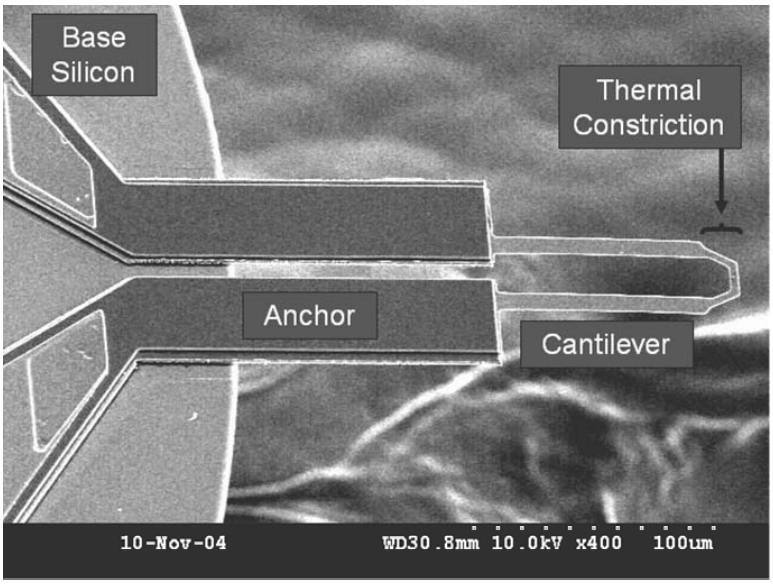


Figure 7. SEM of base silicon, anchor, cantilever and thermal constriction.

The anchor that connects the cantilever to the base silicon creates a fabrication and an application advantage. During fabrication a deep reactive ion etch (DRIE) releases the cantilever from the base silicon. This etch is not consistent across a wafer and over etches some areas while under etching others. When only the cantilever extends from the base silicon, this inconsistency leads to cantilevers of different lengths across a single wafer. Instead, if an anchor connects the cantilever to the base silicon, the variation in etch rate is accounted for by releasing not only the cantilever but ideally half of the anchor as well. Thus any variations in etch rate across the wafer does not effect the resulting cantilever length, but effects the resulting anchor length. The anchor is approximately 4 times thicker than the cantilever which makes the anchor stiffness more than 10 times that of the cantilever stiffness. For imaging purposes the variation in the

stiffness between the anchor and the cantilever should not influence the cantilever imaging capability.

The anchor addition leads to an additional advantage when using the heated AFM cantilever in a conventional AFM instrument. With most AFM applications it is necessary to reflect a laser off the backside of the cantilever, thus requiring that the cantilever protrude from the base silicon by a specific amount. The anchor extension distance depends upon the base silicon thickness, the angle at which the cantilever is held with respect to the imaging surface, and the required cantilever length. Thus, with the anchor addition the effective cantilever length is increased by 100µm and allows greater laser access to the top surface of the cantilever. Figure 8 demonstrates the both situations, without and with the anchor.

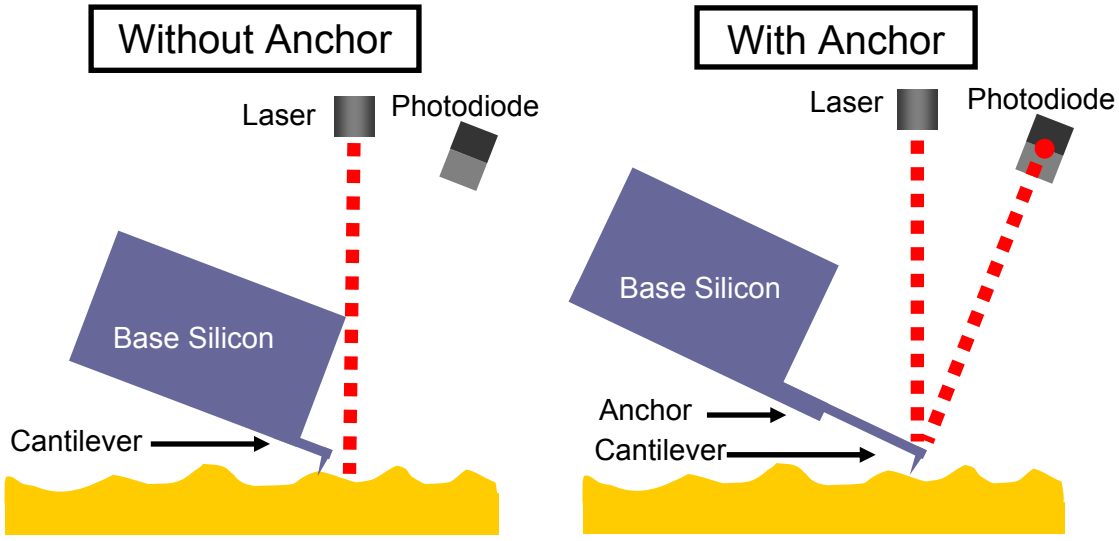


Figure 8. Cantilever accessibility with the laser is greatly increased with the addition of an anchor.

3.1.3 Final Heated AFM Cantilever Designs

Six different cantilever designs, labeled A-F, fill a 10mm by 10mm area. A pattern of this 100mm^2 area produces 75 cantilevers of each design per wafer, or 450 individual devices. Table 1 lists the six cantilever designs and their mechanical properties. The mechanical properties were calculated assuming that the cantilever thickness was 1μm. Figure 9 shows the 6 cantilever designs. Appendix B shows the mask designs used for fabrication.

Table 1. Physical dimensions and mechanical properties for heated AFM cantilevers of 1μm thickness.

Beam	**Heater Width (μm)**	**Heater Length (μm)**	**Leg Width (μm)**	**Leg Length (μm)**	**Cantilever Mass (kg)**	**Spring Constant (N/m)**	**Natural Frequency (kHz)**
A	5	10	10	100	4.78e-12	0.48	515
B	5	10	10	150	7.11e-12	0.14	230
C	5	10	15	150	1.06e-11	0.21	230
D	8	16	10	100	4.96e-12	0.48	505
E	8	16	15	150	1.08e-11	0.21	228
F	8	16	15	150	1.08e-11	0.21	228

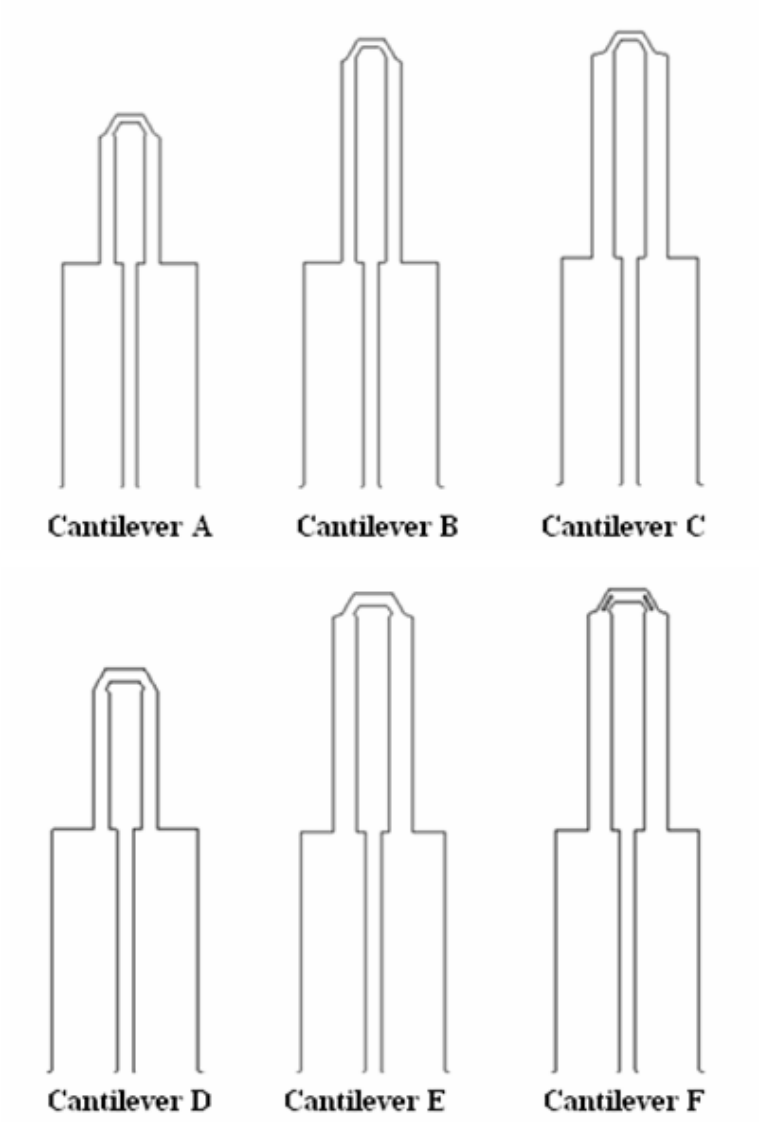


Figure 9. Final cantilever designs A-F.

Cantilevers E and F match in dimension but vary by the addition of cutouts in the thermal constriction area of cantilever F. The cutouts further restrict the heat flow from the tip to the cantilever legs. Figure 10 is an SEM of cantilever F and shows the cutouts. The addition of thermal constrictions to the final cantilever design aids in the cantilever thermal efficiency. By reducing the amount of material between the heater and the

cantilever legs, effectively creating a heat flow constriction, the cantilever heating and cooling becomes more efficient. The reduction in mass decreases the thermal time constant of the cantilever.

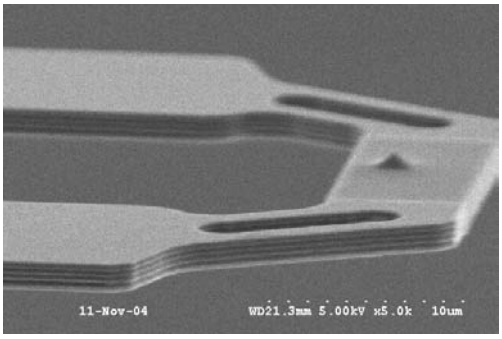


Figure 10. Cantilever F. Note cutouts in the thermal constriction region.

3.2 Cantilever Fabrication

Fabrication of heated AFM cantilevers follows five steps; 1) tip formation, 2) cantilever formation, 3) electrical activation, 4) metallization, and 5) cantilever release. In the following sections the fabrication process is detailed. Figure 11 shows a breakdown of the five fabrication steps along with an expanded description of each phase. Specific processing details are included in spreadsheet form in Appendix A.

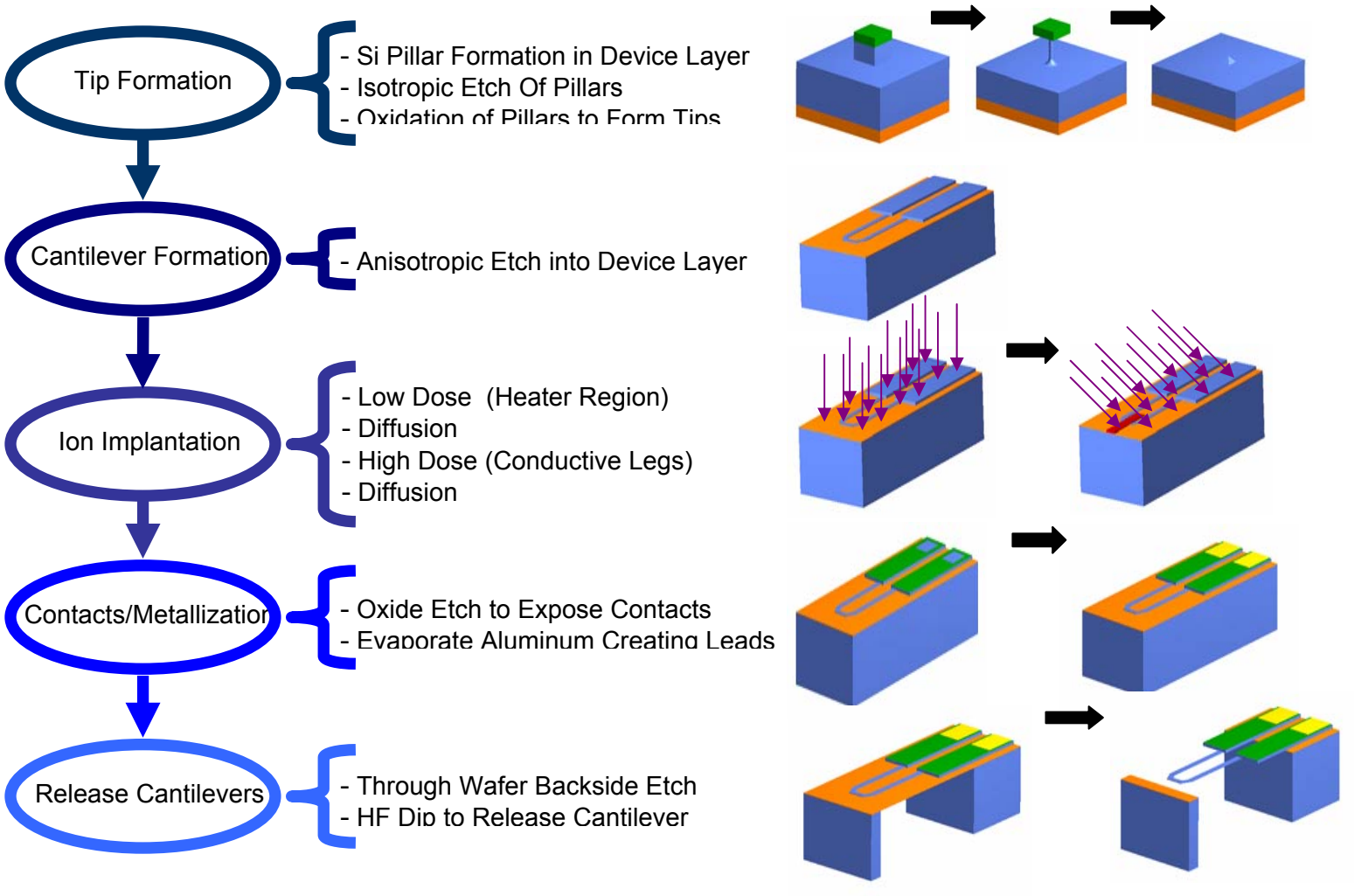


Figure 11. Five step breakdown of the fabrication process.

Fabrication starts with an n-type <100> double side polished silicon on insulator (SOI) wafer with a device layer thickness of 5μm, a buried oxide layer of 1μm, a resistivity of 1 – 10 Ω-cm, and a doping concentration of 1e14 Ω/cm^3. Before processing, an ellipsometer takes multiple thickness measurements and the minimum device layer thickness is established. This minimum thickness determines the necessary etching depth, specifically during the tip creation process. Failure to find this thickness and using it in the etching depth calculation results in portions of the device layer being entirely removed during future etching steps.

3.2.1 Step 1: Tip Formation

Tip formation is divided into three steps: 1) pillar formation with an anisotropic silicon etch into the device layer, 2) isotropic silicon etch to undercut the silicon dioxide cap and thin the pillars, and 3) oxidation sharpening of the thinned pillars to create the final tip structures.

Figure 12 shows these steps and Appendix B1 contains a diagram of the masks used during fabrication.

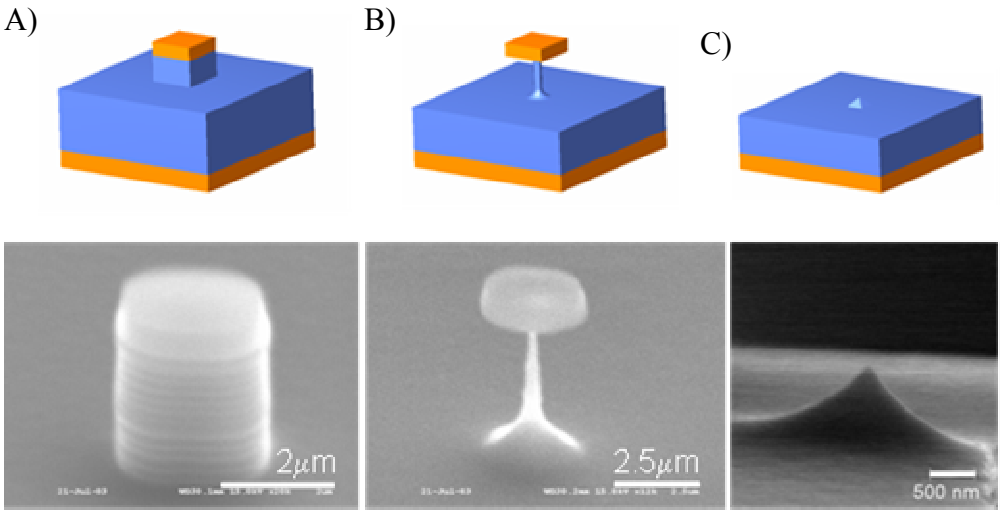


Figure 12. Oxidation sharpening process – cartoon and SEM. A) Anisotropic etch of device layer to create pillar. B) Isotropic etch of pillar to create thin pillar. C) Atomically sharp tip after post oxidation sharpening.

A plasma enhanced chemical vapor deposition (PECVD) machine deposits 5000Å of silicon dioxide onto the front and back sides of the wafer. This oxide layer protects the back side and serves as a mask for the front side of the wafer. A thin photoresist, Shipley 1813, is spun onto the wafer and the first photolithography step defines the cantilever tip, and the device anchor and base regions. After developing the photoresist the wafer is put into the Plasma-Therm Inductively Coupled Plasma (ICP) etcher to dry etch the photoresist pattern into the silicon dioxide. A Bosch process in the Surface Technology Systems (STS) ICP etcher transfers the silicon dioxide pattern into the device layer. Approximately 6 cycles are necessary to etch 1.5μm into the device layer. The resulting tip feature in the device layer is a 2.5μm by 2.5μm silicon pillar that is roughly 1.5μm tall with a silicon dioxide cap, such as in

Figure 12A, along with a defined anchor and base region.

A piranha clean (H_2SO_4:H_2O_2 :: 3:1) strips the wafer of the photoresist mask and prepares the wafer for the isotropic silicon wet etch in HNA. HNA etches 1μm of the silicon pillar while undercutting the silicon dioxide cap until only a 0.5μm thick silicon pillar and oxide cap remain, see

Figure 12B.

3.2.1.1 Isotropic Etch: HNA

HNA is an isotropic etchant consisting of hydrofluoric acid (HF), nitric acid (HNO_3), and acetic acid (CH_3COOH). At different ratios this acid combination etches silicon from 4+ μm/min (HF:HNO_3:CH_3COOH :: 1:7.5:3) to 0.7 μm/min (HF:HNO_3:CH_3COOH :: 1:3:8) and etches oxide at a rate of 0.07 to 0.03 μm/min respectively. Chemically, the nitric acid oxidizes the exposed silicon, the hydrofluoric acid etches the oxide, and the acetic acid stabilizes the reaction [15].

The control and uniformity of HNA lent itself well to this particular application when compared to dry etching techniques such as using a Reactive Ion Etcher (RIE) or ICP. Control of the HNA etch stems from the relatively low etch rate of this particular combination of acids.

The chosen concentration of HNA lends itself to manual processing since small errors in the amount of time the wafer is submerged in the HNA will not have dramatic effects on the resulting features. Uniformity of the etch increases by agitating the wafer during submersion in the HNA. Agitation assists in the transport of fresh reactive species of HNA to the etching surface.

For tip formation HNA (HF:HNO_3:CH_3COOH :: 1:3:8) thins the silicon pillar by 1μm on each side. The HNA etches silicon at a faster rate when compared to oxide thus

undercutting the oxide. Resulting from this etch is a thin pillar of silicon approximately 0.5μm in width. The cantilever anchor and device base are also etched during this step but due to their large size their overall dimensions are only slightly decreased.

3.2.1.2 Oxidation Sharpening

Atomically sharp tips can be fabricated through the silicon oxidation [16]. One of the most critical processing steps, the silicon pillar oxidation defines the final height and radius of curvature of the tip which in turn determines the cantilever imaging resolution.

The oxidation of a planar silicon surface can be modeled by two different regimes. During the initial regime oxygen reacts with exposed surface silicon to create a thin silicon dioxide layer, often called native oxide. This reaction occurs linearly until a critical oxide thickness is achieved. The critical oxide thickness is a function of oxidation pressure and temperature. Upon reaching the critical thickness the oxidation process changes from a linear regime to a parabolic regime. In this second regime the oxygen molecules must diffuse through the existing oxide layer to react with the silicon below.

At high temperatures, 900°C to 1200°C, the introduction of wafer vapor into the oxidation process increases the oxygen diffusion though the existing oxide. Above 900°C the water vapor solubility in silicon is much higher than the solubility of pure oxygen thus increasing the silicon oxidation rate.

During oxidation silicon is consumed and chemically transformed into silicon dioxide. Approximately 54% of the resulting oxide layer lies above the original silicon surface while the remaining 46% of the oxide layer is created from the consumption of the original silicon surface [17]. Figure 13 illustrates this process.

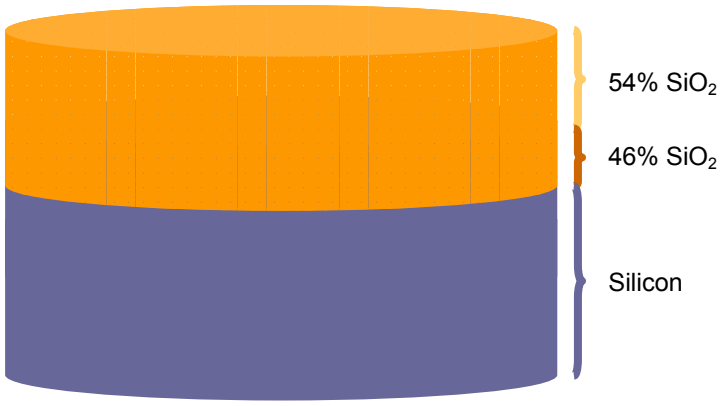


Figure 13. Of the final oxide thickness ~46% is generated from the original silicon surface and ~54% is new oxide.

The oxidation of a feature that is composed of high curvature regions, for example the square pillar that begins tip formation, does not follow the two regimes discussed above [16]. Regions of high curvature are zones of high stress, and during oxidation the silicon consumption in these high stress zones decreases 30% at temperatures below 1050°C. This decrease is the result of a specific volume difference between the silicon dioxide with respect to the silicon. At temperatures below 1050°C the oxide viscosity is appreciable which in turn generates stresses within the oxide. These stresses suppress the silicon/oxygen interfacial reaction which leads to the reduction in oxidation rate. For oxidation temperatures greater than 1050°C the oxide viscosity reduces allowing the oxide to flow. This flow relieves the previous stress buildup and recovers the 30% decrease of silicon consumption, as shown in

Figure 14.

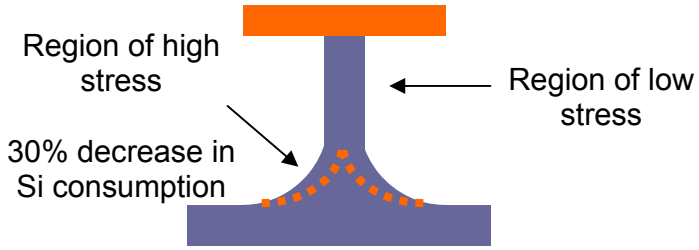


Figure 14. Pillar oxidation to form sharp cantilever tip. Uses geometry induced stresses to decrease oxidation in areas of high curvature.

For this study the tip is created through the oxidation of a thin silicon pillar that is approximately 0.5μm in width. At the pillar base is a region of high curvature and high stress. Wet oxidation of this thin pillar at 950°C for 4 hours utilizes the varying oxidation rates induced by the feature geometry, i.e. the oxidation rate at the base of the structure is slower than the rate at the middle of the pillar. After sufficient time the silicon consumed through oxidation in the planer region of the pillar will meet the oxidation from the other parallel planer regions. This curved oxidation front creates the cantilever tip.

Post oxidation, BOE (Buffered Oxide Etch 6:1) removes the thermally grown oxide revealing the tip. To ensure that the tip formation is complete, wafer examination is done in an SEM (Scanning Electron Microscope). If the tip is not fully formed the oxidation and BOE steps can be repeated.

3.2.2 Step 2: Cantilever Formation

The second step in cantilever fabrication is to pattern and etch the remaining device layer to create the physical cantilever structure. A photolithography step defines the cantilever, anchor, and base device structures into the photoresist, and a 30 second dry oxide etch in the PT ICP removes any native oxide on the exposed device layer. The

wafer is transferred to the STS ICP where a fluorine based Bosch process etches the remaining silicon device layer until the buried oxide layer is exposed, see Figure 15. Appendix B2 has a diagram of the photolithography mask used in this step.

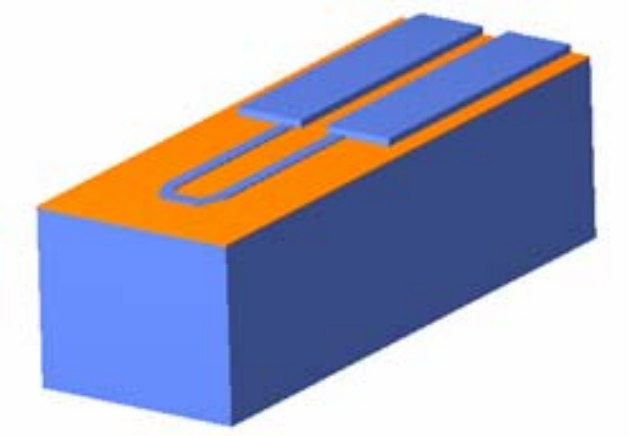


Figure 15. Anisotropic silicon etch through device layer to create silicon cantilever.

It should be noted that post tip formation the anchor and base are still at the original device layer thickness while the thickness of the device layer that creates the cantilever has been thinned during previous processing. Thus, there is a difference in thickness between the cantilever and anchor/base regions. The anchor/base is approximately 4 times the thickness of the final cantilever.

3.2.3 Step 3: Ion Implantation and Diffusion

The transformation of a silicon cantilever into an electrically active device is done by selectively masking, doping, and diffusing impurities into the cantilever. Doping single crystal silicon allows this material to achieve a wide range of electrical resistivity. By selectively masking the silicon different resistivity regions can exist on the same cantilever.

There are two implantation and diffusion steps. During the first implantation 2μm of photoresist protects the bulk silicon at the base of the cantilever but exposes the cantilever heater, legs and anchor to a low dose of phosphorous ions. This implantation creates the high background resistivity necessary in the heater region. Figure 16A and Appendix B3 illustrates this mask design. A 2μm thick photoresist mask protects the heater region and bulk silicon from the second high dose implantation but exposes the cantilever legs and anchor which decreases the resistivity of these regions, Figure 16B and Appendix B4. By selectively masking the heater from the second implantation the resistivity remains high. This results in approximately 90% of the total cantilever resistance being generated in the heater region. After each implantation the wafer is heated to diffuse and activate the dopants into the silicon. Upon completion of these steps the cantilever can carry current though its highly doped/low resistive legs and anchor, and heat as current passes though its low doped/highly resistive heater region. Details of each implantation and diffusion step follow. Dosage calculations are given in Chapter 4 under Diffusion Modeling.

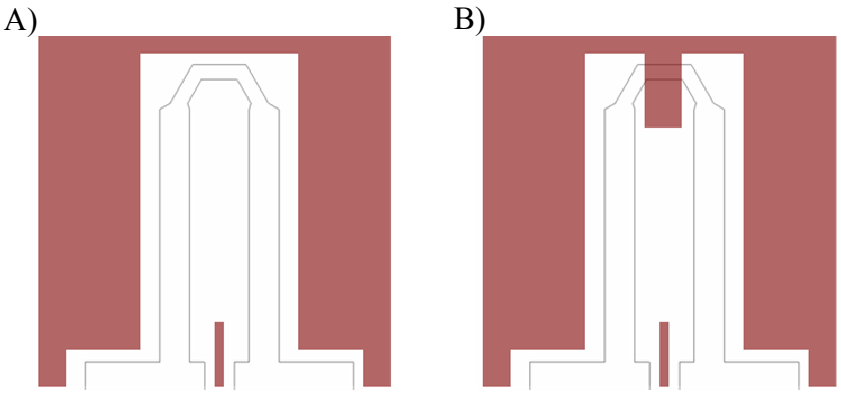


Figure 16. Selective doping masks. A) Low dose implantation mask exposes entire cantilever to low dose implantation. B) High dose implantation mask exposes only the legs and anchor to the high dose implantation. Heater is masked from implantation.

The implantation impurity has an impact on the resulting cantilever electrical properties. Phosphorous was chosen over boron for implantation because at a given doping concentration phosphorous has a higher final resistivity. A higher resistivity has two advantages; it allows power to be delivered to the heater region more efficiently and increases the heated AFM cantilever heating and cooling efficiency.

Before each implantation it is essential that any oxide remaining on the exposed silicon surface be removed with BOE. Post implantation the maximum distribution of impurities will lie only a short depth below the silicon surface, and this depth is dependent upon the implant energy. Any silicon dioxide remaining on the silicon surface reduces the implantation depth by the thickness of that layer [17].

In order to spread the implanted impurities throughout the cantilever thickness the wafer is heated. An oxide cap is deposited onto all wafers post implantation and pre diffusion. If the implanted silicon is not covered with an oxide cap before diffusion the impurities can diffuse into the environment and lower the final silicon volumetric concentration. Ssuprem3 simulations were used to determine the optimal diffusion times and temperatures, and the results are discussed in Chapter 4.

3.2.3.1 1st Implantation and Diffusion

The purpose of the first low dose implantation and diffusion is to create a uniform background resistivity for the entire cantilever and anchor. Because the heater will be masked during further implantations this background doping level, combined with the heater geometry, establishes the heater region resistance. For this study a cantilever resistance of approximately 2000Ω was desired. To obtain this resistance a final background volumetric concentration of 1e17 atoms/cm^3 is necessary given the heater

geometry and thicknesses ranging from 0.5 – 1.25 μm. The combination of these parameters results in a heater resistance from 1120 – 2800Ω respectively.

To maximize implantation depth BOE is used to strip the cantilever structure of any remaining oxide. The wafer is covered with Shipley 1827 photoresist and patterned to expose the anchor, legs, and heater region of the cantilever. An external implantation vendor implants a low dose of phosphorous ions (2.51e13 atoms/cm^2) into the wafer at a 7° angle and at an 200keV energy level, see Figure 17. At this dosage and energy level the bulk of the phosphorous dopants are embedded 3000Å deep in the silicon.

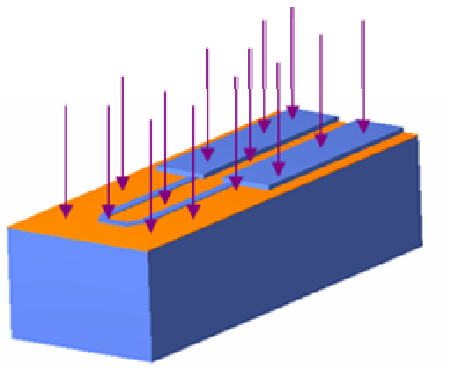


Figure 17. Low dose phosphorous implantation, entire cantilever is exposed and implanted at a 7° angle.

To activate the implanted phosphorous it is necessary to diffuse the impurities throughout the cantilever thickness. Before diffusion, though, piranha removes the photoresist mask and the STS PECVD deposits 1000Å of oxide over the exposed cantilever. After deposition, heating the wafer at 1000°C for 0.5 hours in a nitrogen environment minimally diffuses the phosphorous into the silicon. This diffusion step is only preliminary. After the second high dose implantation another diffusion step further drives both the low and high dose implantations to their optimal volumetric

concentrations, 1e17 atoms/cm^3 for the heater and 1e20 atoms/cm^3 for the legs and anchor. The division of the two diffusion steps is necessary since the phosphorous diffusion coefficient into silicon is dependent upon the implanted dopant concentration. Diffusion rates increase as the impurity concentrations increase.

3.2.3.2 2nd Implantation and Diffusion

The objective of the second implantation and diffusion is to implant and diffuse phosphorous into the cantilever legs and anchor only. A high dose of phosphorous ions (2.51e16 atoms/cm^2) transforms the silicon in these parts into a highly conductive material. Post diffusion, the final volumetric concentration of the cantilever legs and anchor is close to 1e20 atoms/cm^3. By design, the high impurity concentration in these areas extremely decreases their resistivity thus constraining the heater region to comprise nearly 90% of the total cantilever resistance.

To prepare the wafer for the second implantation it is necessary to remove any oxide on the silicon surface with BOE. Shipley 1827 covers the wafer and is optically patterned such that the photoresist covers the heater while the cantilever legs and anchor remain exposed. An outside vendor implants the phosphorous into the wafer, this time at a surface concentration of 2.51e16 atoms/cm^2, at 200KeV, and at a tilt angle of 45°. Tilting the wafer during implantation is necessary in order to electrically active the silicon sidewall that connects the anchor to the cantilever legs. There exists a maximum height difference of 4μm between the top surface of the anchor and the top surface of the cantilever legs as shown in Figure 18A. In order for a current to travel through the anchor to the cantilever legs an electrical path must exist between these two planes along the anchor sidewall. Implanting the phosphorous at a 45° angle with respect to the top of

the wafer ensures electrical path creation. Figure 18B demonstrates the implantation at a 45° angle.

A) B)

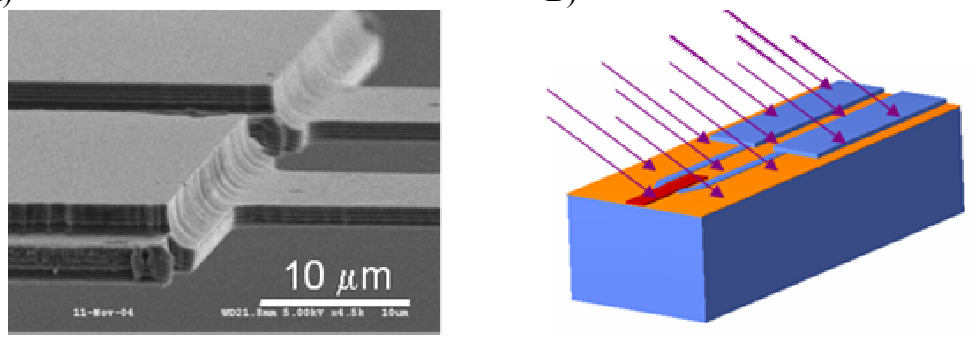


Figure 18. A) High dose phosphorous implantation, heater region is covered in photoresist, implanted at a 45° angle. B) 45° angle implantation will implant into the side wall of the anchor.

Post doping, subsequent piranha and asher treatments clean the patterned photoresist from the wafer and then the STS PECVD deposits an oxide layer of 1000Å onto the silicon. This oxide layer is necessary for two reasons. First, the layer creates a barrier that traps the implanted dopants in the silicon during the diffusion step. Secondly the layer acts as an isolator between the doped silicon and the metal leads that will be fabricated in the following step. The wafer with protective oxide cap is then put into a furnace at 1000°C for 2 hours to complete the dopant diffusion.

3.2.4 Step 4: Contact Formation and Metal Lift-Off

At this point the cantilever is electrically active and requires metal leads to join the active silicon with the base of the device. A thin oxide layer covers the doped silicon and acts as an isolative layer between the metal leads and the doped silicon. In order to electrically connect to the doped silicon, though, holes in the oxide layer are necessary.

Shipley 1827 is spun onto the wafer and photo lithographically patterned, resulting in the exposure of only the areas needed for contact between the metal and doped silicon. Dry etching the wafer in the ICP removes the exposed insulating layer and uncovers the doped silicon below, as diagramed in Figure 19. A figure of the mask is shown in Appendix B5. Piranha removes the remaining photoresist and the wafer is ready for the next photolithography step.

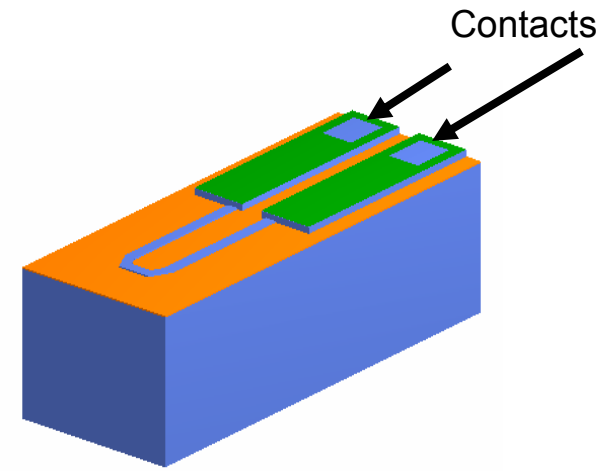


Figure 19. Open contacts in oxide layer expose doped silicon.

Due to large feature sizes, metal liftoff was chosen for metal patterning rather than a metal deposition/etching step. For adequate sidewall height a thicker negative photoresist (NR7-1500P) is used. NR7-1500P covers the wafer and optical lithography patterns the photoresist resulting in the exposure of the device leads. A figure of this mask is given in Appendix B6. These leads create the electrical connections between the doped silicon and the pads necessary for wire bonding at the base of the device. A 15 second dip in BOE immediately before metallization removes any native oxide in the newly formed contact areas. The wafer is then put into an e-beam evaporator for

metallization. Evaporation of 7000Å of aluminum onto the wafer surface covers all areas perpendicular to the evaporation, including the contact holes, but does not cover the tall sidewalls of the photoresist.

The wafer is placed in a warm (80°C) photoresist stripper (RR2) bath for 20 minutes. RR2 attacks the photoresist through the exposed sidewalls and lifts-off any aluminum covering the photoresist, thus leaving aluminum in the areas that did not have photoresist, Figure 20. After rinsing and drying the wafer, an ohm meter electrically verifies that contacts exist been the doped silicon and the wire bond pads. To further enhance the contact between the doped silicon and the deposited aluminum a 30 minute annealing process at a temperature of 400°C in an inert atmosphere is completed. Although 400°C is well below the eutectic temperature for silicon and aluminum (577°C) the aluminum is absorbed into the silicon decreasing any contact resistance due to impurities or oxide that may have been left on the surface. Pre sintering, the average resistance was 7.7kΩ. Post sintering, the resistance dropped to 1.17kΩ. Thus sintering decreased the average contact resistance by approximately 6.53kΩ.

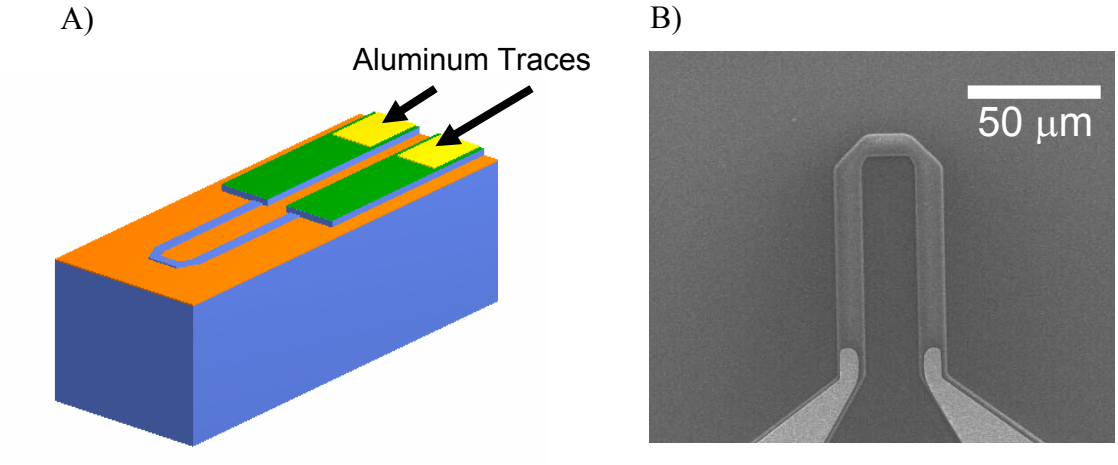


Figure 20. Metallization and lift-off to create aluminum contacts with doped silicon. A) Pictorial representation of metallization. B) SEM of aluminum contacts.

3.2.5 Step 5: Through Wafer Etch

If electrical testing yields favorable results the wafer is prepped for the backside silicon etch. A thick photoresist (AZ4620) is spun onto the wafer at a thickness of 15μm and hard backed for 5 minutes at 115°C to protect the top side features during the deep RIE (DRIE) etching. A similar photoresist layer covers the backside of the wafer. Optical lithography patterns windows onto the backside of the wafer such that they are aligned with the cantilevers on the front side. Appendix B7 has a diagram of this mask.

Before etching the backside in the PT ICP the wafer is placed on a dummy wafer that has been coated with a thick photoresist and the combination is cured on a hotplate. Post curing, the PT ICP removes any residual oxide from the exposed features on the backside of the wafer.

At this point the wafer is transferred into a separate chamber in the PT ICP where the Bosch process etches silicon at approximately 0.5μm/cycle. For a 550μm thick wafer

approximately 1100 cycles are necessary to fully etch through the entire wafer. After 1000 cycles have been completed the wafer is screened after every 100 cycles are completed. The backside etch should be stopped when etching reveals the buried oxide layer in all open areas, Figure 21. The oxide layer is translucent and the cantilevers from the front side of the wafer can be seen in the open areas. Etching can be very non-uniform across the wafer and thus some cantilevers will be observed before others. Over etching during this step can damage the silicon cantilevers that have already been exposed.

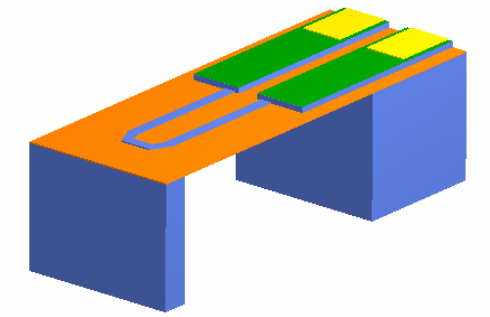


Figure 21. DRIE through backside of handle wafer until buried oxide layer is exposed.

Once the backside etch is complete submersion of the wafer and holder into a warm bath of AZ400T stripper removes the photoresist and separates the two parts. Upon separation the wafer is lightly rinsed and then dried on a hot plate at 100°C. Using nitrogen to dry the fragile wafer at this point may break the thin 1μm oxide membrane that is holding the cantilevers into the wafer.

A 15 second dip in 49% HF etches the thin oxide membrane and releases the cantilevers from the wafer. The final devices are snapped out of the supporting wafer and imaged in the SEM. An example of a cantilever and tip are shown in Figure 22 A and B.

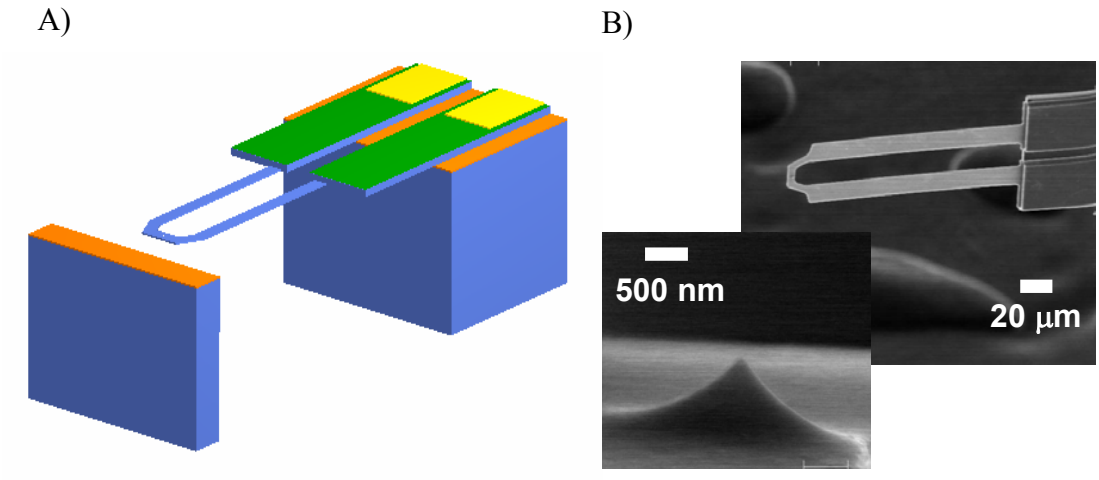


Figure 22. Final heated cantilever. A) Pictorial representation. B) SEM images of the tip and the cantilever.

Post fabrication and before experimental testing the cantilevers are separated from the wafer and imaged in an SEM. From the SEM images geometry and thickness approximations are resolved and will be used in future theoretical simulations. To date the Georgia Institute of Technology is the third place in the world to create thermal cantilevers, only behind IBM Zurich and Stanford University.

CHAPTER IV

MODELING HEATED AFM CANTILEVERS

This chapter describes the thermal and electrical simulations of the heated AFM cantilever. To simplify the discussion this chapter is divided into two sections: 1) modeling the thermal and electrical response, and 2) detailed impurity diffusion modeling using Ssuprem3. Only the steady state response of the cantilever will be discussed, although the simulation can be easily modified for transient situations.

The theoretical model captures the close coupling between the thermal and electrical response of the cantilever. Two regions exist within the cantilever, the highly doped conductive legs and the lightly doped resistive heater, which is located at the free end of the cantilever. The cantilever is placed in series with a resistor, often referred to as the sense resistor, of resistance approximately equal to the cantilever resistance. A voltage applied across the circuit generates a current that induces resistive heating in the highly resistive lightly doped heater. The heat generated conducts to and warms the cantilever legs and also thermally reacts with the environment. Depending on how close the cantilever is to another surface the environmental heat transfer effects may be negligible when compared to the conduction of heat through the cantilever legs. The resistivity of doped silicon is temperature dependent and therefore changes with the cantilever temperature. A change in cantilever resistivity can be monitored through voltage measurements across the sense resistor. Figure 23 is a circuit schematic.

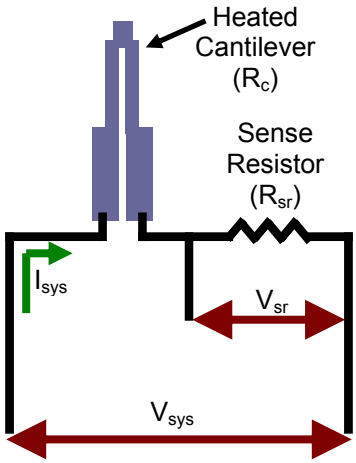


Figure 23. Heated AFM cantilever/sense resistor circuit.

4.1 Thermal and Electrical Model

The study of the heat generation within and flow through the cantilever and its connection to the silicon temperature dependent electrical properties are at the core of this project. The model created simulates these interactions and combines heat transfer fundamentals, finite difference methods and basic electrical circuit theory. The simulation explanation is divided into three sub-sections: the 1) heat flow control volume analysis, 2) numerical approach, and 3) the link between the electrical and theoretical model.

Figure 24A shows a heated AFM cantilever illustration. Heated AFM cantilevers are symmetric and therefore, for simplicity, only half of the cantilever was modeled. The modeled symmetry requires an adiabatic boundary condition at the free end, or heater region, of the cantilever.

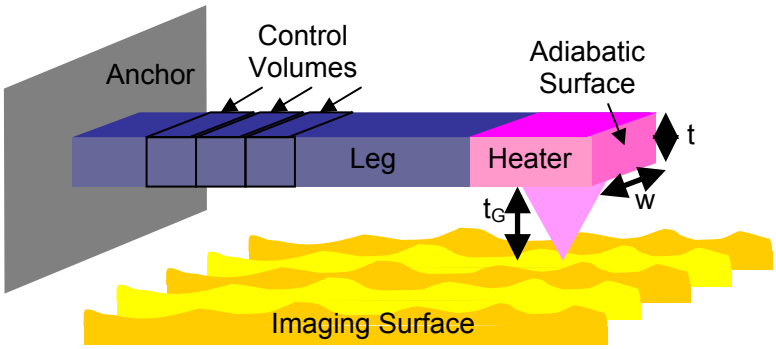


Figure 24. Physical interpretation of modeled cantilever.

The model created divides the cantilever into control volumes of equal length and applies a thermal energy balance to each control volume. An implicit finite difference method solves for the temperature at each node. Each calculated node temperature is then related to the electrical response of the cantilever through the temperature dependent properties of silicon. Iteration occurs until a final steady state temperature solution is achieved.

4.1.1 Thermal Model – Control Volume Analysis of Heat Flow

An energy balance at each control volume accounts for the energy entering and leaving the volume, see Figure 26 and equation (4.1). This equation describes the energy balance in terms of q_R, q_L, q_S, q_E., q_{stored} and $q_{generated}$. Each term describes the heat transfer to the right, left, substrate, and environment respectively, which the q_{stored} and $q_{generated}$ are the internally stored and generated heat.

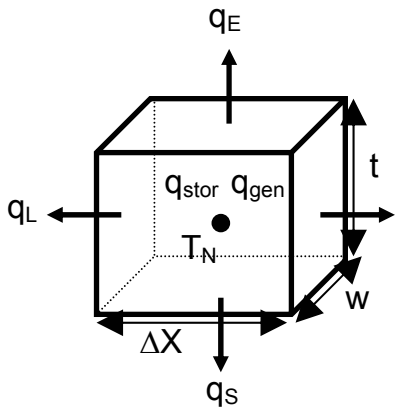


Figure 25. Thermal energy balance on one control volume element.

$$q_L + q_R + q_S + q_E = q_{Stored} - q_{Generated} \tag{4.1}$$

Conduction is the principal heat transfer mode along the length of the cantilever. Conduction, convection, and radiation were all assumed to be pertinent heat transfer modes between the cantilever and the substrate, while only convection and radiation were assumed to influence the heat transfer between the cantilever and the environment. Figure 26 shows a diagram of these three heat transfer modes with respect to the modeled cantilever.

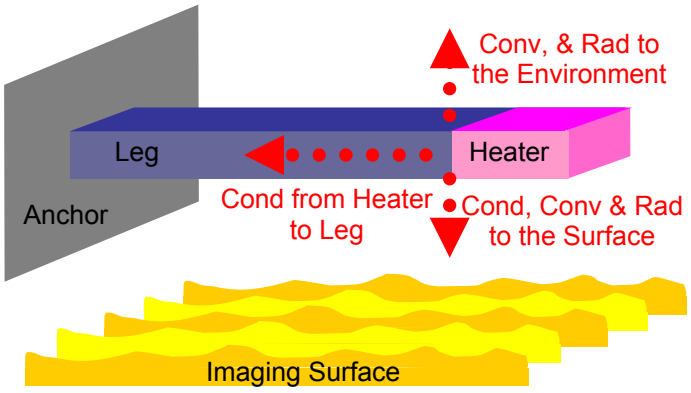


Figure 26. Heat transfer from the heated AFM cantilever.

Fourier's Law models the conduction heat transfer entering and leaving the control volume from the left (L) and right (R). Equations (4.2) and (4.3) describe this relationship where $k_{L,R}$ is the thermal conductivity of silicon to the left or right, $T_{N,L,R}$ is the temperature at the node, left or right, t is the cantilever thickness, w is the cantilever width, and Δx is the length of the control volume.

$$q_L = \frac{k_L(T_N)\cdot t\cdot w}{\Delta x}(T_N - T_L) \tag{4.2}$$

$$q_R = \frac{k_R(T_N)\cdot t\cdot w}{\Delta x}(T_N - T_R) \tag{4.3}$$

The flow of heat from the cantilever to its surroundings is modeled by conduction, convection and radiation. The equation describing the conduction between the cantilever and a surface is given in (4.4). In the equation k_{air} represents the thermal conductivity of the air and t_g is the distance between the cantilever and the surface.

$$q_{cond} = k_{air}(T_N - T_S)\frac{w\cdot\Delta x}{t_g} \tag{4.4}$$

Equation (4.5) describes the convection between the cantilever and the environment. The symbol h_{air} describes the convection coefficient of the air.

$$q_{conv} = h_{conv}(T_N - T_E)w\cdot\Delta x \tag{4.5}$$

The previously stated conduction and convection heat transfer equations are linear, while the radiation equation (4.6) is non-linear due to a T^4 temperature term. The ε in equation (4.6) represents the emissivity of silicon, the σ represents the Stefan-Boltzmann constant, and the T_E term represents the environment temperature.

$$q_{rad} = \varepsilon\sigma(T_N{}^4 - T_E{}^4) \tag{4.6}$$

For convergence stability within the program a lineraized radiation equation (4.7) is used rather than the widely recognized radiation equation. The nonlinear T^4 term of

equation (4.6) keeps the radiation contribution from easily being substituted into the chosen numerical solution scheme. By using the linearized equation and its radiation heat transfer coefficient, (4.8), the numerical method easily integrates the radiation component into the solution. During each iteration the radiation heat transfer coefficient, h_{rad}, is updated with the node temperature from the previous iteration, T_N^{t-1} where t-1 represents the previous iteration step. The radiation coefficient is also subbed into the linearized equation during each iteration, which when equations (4.7) and (4.8) are mathematically combined give you equation (4.6).

$$q_{rad} = h_{rad}(T_N - T_E)w \cdot \Delta x \tag{4.7}$$

$$h_{rad} \equiv \varepsilon\sigma(T_N^{t-1} + T_E)((T_N^{t-1})^2 + T_E^{\,2}) \tag{4.8}$$

Equations (4.9) and (4.10) combine the three heat transfer modes to describe the heat flows from the top and bottom surface of the cantilever respectively.

$$q_E = h_{air}(T_N - T_E)w \cdot \Delta x + h_{rad}(T_N - T_E)w \cdot \Delta x \tag{4.9}$$

$$q_S = h_{air}(T_N - T_E)w \cdot \Delta x + h_{rad}(T_N - T_S)w \cdot \Delta x + k_{air}(T_N - T_S)\frac{w \cdot \Delta x}{t_g} \tag{4.10}$$

For completeness the time dependent storage term has been included, but all simulations in this study set the time step, $d\theta$, to a very large number thus removing any influence of the energy storage term from the simulations. All simulations are steady state. Equation (4.11) illustrates this q_{stored} term where ρ is the density, c is the specific heat, and v is the volume of the differential element.

$$q_{stored} = \rho \cdot c \cdot v\frac{dT}{d\theta} \tag{4.11}$$

The heat generated, $q_{generated}$, is a function of the power generated in the cantilever during use, see equation (4.12). This equation has a strong dependence on the electrical

response of the cantilever, this term will be discusses in more detail during the electrical modeling section of this chapter.

$$q_{generated} = I^2 R_{node} \tag{4.12}$$

The thermal conductivity of the silicon is a function of temperature and the impurity density implanted into the silicon. In both cases there is an inverse relationship with temperature. At present there is limited data on the thermal conductivity of doped, thin silicon layers. This study extracts thermal conductivity data from the thesis presented by B. Chui, 1998 [18]. Equations (4.13) and (4.14) represent the temperature dependent thermal conductivity for the leg and heater components respectively.

$$k_{leg}(T_N) = 100302 \cdot T_N^{-1.2023} \tag{4.13}$$

$$k_{htr}(T_N) = 122975 \cdot T_N^{-1.206} \tag{4.14}$$

Table 2 lists all constants, symbols, values, and units for each equation given in Chapter 4. The value for the thermal conductivity of air, k_a, was taken from a standard heat transfer text book [19], while the environmental convection coefficient, h_E, was taken from a paper which discusses modeling the thermal runaway effect associated with heated AFM cantilevers [20].

Table 2. Symbols and constants used in heat transfer equations.

Ht Trans Term	Symbol	Variable Name	Value	Units
Conduction (q_L, q_R)	$T_{N,L,R}$	Node, left, or right temperature	Variable	K
	w	Cantilever width	Variable	μm
	t	Cantilever thickness	Variable	μm
	Δx	Width of control volume	0.5	μm
	$k(T_N)$	Thermal conductivity – function of T_N	N/A	W/mK
Conduction (q_E, q_S)	T_N	Node temperature	Variable	K
	$T_{E,S}$	Environment and substrate temperature	300	K
	w	Cantilever width	Variable	μm
	Δx	Width of control volume	0.5	μm
	t_g	Distance between cantilever and substrate	550	μm
	k_b	Thermal conductivity of base	148	W/mK
	k_a	Thermal conductivity of air	0.02	W/mK
Convection (q_E, q_S)	T_N	Node temperature	Variable	K
	$T_{E,S}$	Environment and substrate temperature	300	K
	w	Cantilever width	Variable	μm
	Δx	Width of control volume	0.5	μm
	h_E	Environment convection coefficient	0.1	W/m^2K
Radiation (q_E, q_S)	T_N	Node temperature	Variable	K
	$T_{E,S}$	Environment & substrate temp	300	K
	ε	Emissivity	0.95	N/A
	σ	Stefan-Boltzmann constant	5.67e-8	W/m^2K^4
	h_{rad}	Linearized radiation coefficient	Variable	W/m^2K
Storage ($q_{Storage}$)	T_N	Node temperature	Variable	K
	$T_{E,S}$	Environment & substrate temp	300	K
	ρ	Density of silicon	2330	kg/m^3
	c	Specific heat of silicon	712	J/kg K
	v	Volume of control volume	Variable	μm^3
	$d\theta$	Time step	1e6	sec
Generated ($q_{Generated}$)	q_{gen}	Function of electrical properties	Variable	W

4.1.2 Thermal Model – Numerical Approach

For each node, equations (4.2), (4.3), (4.9) - (4.11), and q_{gen} replace the associated heat flows from the energy balance equation (4.1) thus generating a system of equations that describes the heat flow from the cantilever, equation (4.15). Many of the known terms, T_S, T_E and q_{gen} are collected on the right hand side of the equation, while the unknown T_N terms are collected on the left hand side along with the known T_R, T_L terms. A_L, A_R, A_N, and, C are shown in equations (4.16) - (4.19).

$$-A_L T_L + A_N T_N - A_R T_R = C \tag{4.15}$$

$$A_L = 2 \cdot k_L(T) \frac{w \cdot t}{\Delta x} \tag{4.16}$$

$$A_R = 2 \cdot k_R(T) \frac{w \cdot t}{\Delta x} \tag{4.17}$$

$$A_N = T_N \left(2 \cdot k_R(T) \frac{w \cdot t}{\Delta x} + 2 \cdot k_L(T) \frac{w \cdot t}{\Delta x} + 2 \cdot w \cdot \Delta x \cdot h_{air} + 2 \cdot w \cdot \Delta x \cdot h_{rad} + k_{air} \frac{w \cdot \Delta x}{t_g} + \frac{\rho c v}{\Delta \theta} \right) \tag{4.18}$$

$$C = T_E \left(2 \cdot w \cdot \Delta x \cdot h_{air} + 2 \cdot w \cdot \Delta x \cdot h_{rad} + \frac{\rho c v}{\Delta \theta} \right) + T_S \left(k_{air} \frac{w \cdot \Delta x}{t_g} \right) - q_{gen} \tag{4.19}$$

Equation (4.15) describes the energy balance of a cantilever node. Modification of this equation is necessary for the base node and the last node at the end of the heater. Special boundary conditions apply at these two locations.

Where the cantilever joins the anchor, a shape factor boundary condition, S, accounts for the difference in cross sectional area between the cantilever and the anchor [19] and is described by equation (4.20). This heat equation for the node at the base of the cantilever and is used in place of q_L at the base node.

$$q_{L,base} = S k_L \Delta T = 2\sqrt{tw} k_L \Delta T \tag{4.20}$$

The energy balance for the last node in the heater is modified to account for the adiabatic boundary condition. This boundary condition removes the heat term entering the control volume from the right (q_R).

All n nodes of the cantilever can be described by n (4.15) equations and the system of equations is put into matrix form (4.21). The number of rows in this matrix represents the total number of nodes along the cantilever length, where the 1st row corresponds to the node at the base of the cantilever and the last row corresponds to the last node in the heater region. The tri-diagonal A matrix contains the right, node, and left coefficients, A_R, A_N, and A_L, corresponding to the known right, unknown node and known left temperature in the T matrix. The C matrix contains the remaining known terms.

$$\begin{bmatrix} A_N & A_R & 0 & 0 & 0 & \cdots & 0 \\ A_L & A_N & A_R & 0 & 0 & \cdots & 0 \\ 0 & A_L & A_N & A_R & 0 & \cdots & 0 \\ \vdots & & & & & & \vdots \\ 0 & 0 & 0 & \cdots & 0 & A_L & A_N \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_{n-1} \\ T_n \end{bmatrix} = \begin{bmatrix} C_1 \\ C_2 \\ \vdots \\ C_{n-1} \\ C_n \end{bmatrix} \tag{4.21}$$

Simulation begins by guessing an initial temperature at each node and fixing the environment, bulk silicon, and surface below the cantilever at 300K. The initialized system of equations is solved simultaneously for each node temperature. After the first iteration the resulting node temperatures are compared against convergence criteria. The absolute value of the difference between the new and old temperatures is divided by the original temperature and must be less than 0.003 in order for the solution to be considered converged. New node temperatures are calculated with equation (4.22) and are passed to the next iteration loop.

$$T_{new} = T_{old} + 0.5\left|T_{old} - T_{new}\right| \tag{4.22}$$

4.1.3 Electrical Model

The goal of the electrical model is to determine the system current and node resistance as a function of temperature which allows calculation of the heat generated in the cantilever, equation (4.23).

$$q_{generated} = I^2 R_{node} \tag{4.23}$$

The node resistance calculation links the node temperature with the material properties of the silicon. Discussions about the cantilever resistance calculation and its dependence on temperature, electron mobility and cantilever current follow.

4.1.3.1 Electrical Model –Mobility Calculation

The heated AFM cantilever resistivity is temperature dependent. Resistivity, equation (4.24), is inversely proportional to electron mobility, μ, the charge of an electron, q, and the doping concentration, N.

$$\rho = \frac{1}{q\mu N} \tag{4.24}$$

An empirical mobility model relates mobility and temperature. Equations (4.25) to (4.28) hold for doped silicon in the temperature range of 300 to 700K [21]. Table 3 lists the specific parameters used for phosphorous.

$$\mu = \mu_o + \frac{\mu_L - \mu_o}{1 + \left(\frac{N_D}{C_{r1}}\right)^{\alpha_1} + \left(\frac{N_A}{C_{r2}}\right)^{\alpha_2}} - \frac{\mu_1}{1 + \left(\frac{N_D}{C_{s1}} + \frac{N_A}{C_{s2}}\right)^{-2}} \tag{4.25}$$

$$\mu_L = \mu_{\max}\left(\frac{T}{300}\right)^{-\gamma + c(T/300)} \tag{4.26}$$

$$\mu_o = \frac{\mu_{od} N_D + \mu_{oa} N_A}{N_D + N_A} \tag{4.27}$$

$$\mu_1 = \frac{\mu_{1d} N_D + \mu_{1a} N_A}{N_D + N_A} \tag{4.28}$$

Table 3. Bulk mobility parameters for phosphorous.

Parameters (T_n=T/300K)	**Phosphorous Parameters**
μ_{max} (cm^2/Vsec)	1441
c	0.07
γ	2.45
μ_{od} (cm^2/Vsec)	$62.2*T_n^{-0.7}$
μ_{oa} (cm^2/Vsec)	$132.0*T_n^{-1.3}$
μ_{1d} (cm^2/Vsec)	$48.6*T_n^{-0.7}$
μ_{1a} (cm^2/Vsec)	$73.5*T_n^{-1.25}$
C_{r1} (cm^{-3})	$8.5e16*T_n^{3.65}$
C_{r2} (cm^{-3})	$1.22e17*T_n^{2.65}$
C_{s1} (cm^{-3})	4e20
C_{s2} (cm^{-3})	7.0e20
α_1	0.68
α_2	0.72

4.1.3.2 Electrical Model – Cantilever Resistance Calculation

To further refine the cantilever resistance calculation, simulations were run in Ssuprem3 [22] to evaluate the impurity volumetric concentration throughout the cantilever thickness. Electrical activation of the silicon cantilevers includes a phosphorous implantation and diffusion step. The diffusion step distributes the implanted ions throughout the cantilever thickness. Ssuprem3 simulations, have shown that the volumetric concentration of phosphorous through the cantilever thickness is not uniform. Thus one specific volumetric concentration cannot be used in the resistivity/mobility calculation, equations (4.24) and (4.25) for the volumetric concentration dependent terms N_D and N_A.

To account for this varying concentration profile though the cantilever thickness, each node was divided into 100 slices. Shown in Figure 27, a volumetric concentration, determined though Ssuprem3 simulations, was assigned to each slice. For each slice the volumetric concentration, node temperature, and geometry combine to calculate the slice resistivity.

The resulting resistivity of each slice was then converted to a resistance through equation (4.29), where A_c is the cross sectional area of each slice normal to the current flow though the cantilever. At this point the node can be described by 100 resistors in parallel. To find the equivalent resistance of one node the resistors are added in parallel according to equation (4.30). The final cantilever resistance was found by summing the heater and leg resistances and multiplying the result by two, due to the symmetry of the model. Figure 27 shows this process.

$$R = \rho \frac{l}{A_c} \tag{4.29}$$

$$\frac{1}{R_{tot}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n} \tag{4.30}$$

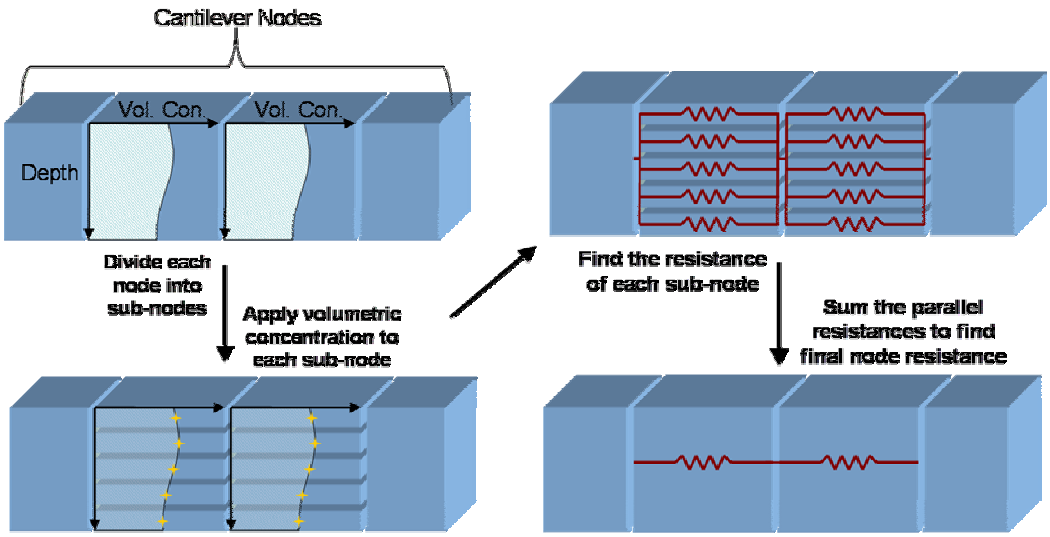


Figure 27. Division of cantilever into sub-nodes though the thickness of the cantilever and application of a variable volumetric concentration.

4.1.3.3 Electrical Model – Current Calculation

To physically characterize a heated AFM cantilever it is put in series with a known sense resistor and the system and sense resistor voltages are monitored, shown in Figure 27. In the theoretical model the system voltage is an input to the program and the cantilever resistance at each node is calculated using the resistivity and mobility models as described in the previous section. To calculate the current flowing through each node equation (4.31) is applied. Where I is the system current, V is the known system input voltage, $R_{cantielver}$ is the resistance of the cantilever, and R_{sense} is the value of the sense resistor.

$$I = \frac{V}{R_{cantilever} + R_{sense}} \tag{4.31}$$

Thus the cantilever resistance at each node and the current though the system are used to evaluate $q_{generated}$. This value is then used in the heat transfer calculations for determining the temperature at each node. Electrical calculations for mobility, cantilever resistance, current and $q_{generated}$ must be found and the new $q_{generated}$ term passed into the heat transfer calculation for each iteration.

4.2 Diffusion Modeling

Heated AFM cantilevers are simple yet clever devices that use selective doping to create different resistive regions within an individual cantilever. The cantilever has two parts, the highly doped conductive legs and the lightly doped resistive heater element, which is located directly above the tip. This section describes how the dopant implantation parameters are determined and the Ssuprem3 modeling of the dopant diffusion.

4.2.1 Dopant Implantation Parameters

CORE SYSTEMS, an outside vendor, selectively implants phosphorous into the silicon cantilevers which transforms the devices into conductive cantilevers. Ion implantation has key advantages over other implantation techniques in that the implantation depth and final surface concentration can be easily controlled during processing. Implantation vendors only need the dopant type, implantation energy, and resulting surface concentration to successfully complete an implantation.

For this study phosphorous was chosen as the implantation species. Phosphorous was chosen over boron as the implantation impurity because at a given dopant concentration a higher electrical conductivity is possible. The enhanced electrical

conduction is an advantage specifically in the legs of the cantilever where current must flow with little resistance.

The energy at which the phosphorus ions are implanted is directly related to the final implantation depth. The higher the energy, the deeper the majority of the ions travel into the silicon. As the implanted ions travel they impact the crystal lattice which slows the majority of the ions to a final depth, designated R_p. Other ions travel either a shorter or longer distance into the silicon which is is designated by ΔR_p. The distribution of the implanted ions in the silicon has a Gaussian distribution. For phosphorous the maximum implantation energy available at the outside vendor was 200keV. This energy results in an implantation depth (R_p) of approximately 2600Å and a spread (ΔR_p) of 896Å. These numbers are taken from Figure 28 at 200keV [17]. Figure 28 shows the projected range of phosphorous impurities as a function of implantation energy.

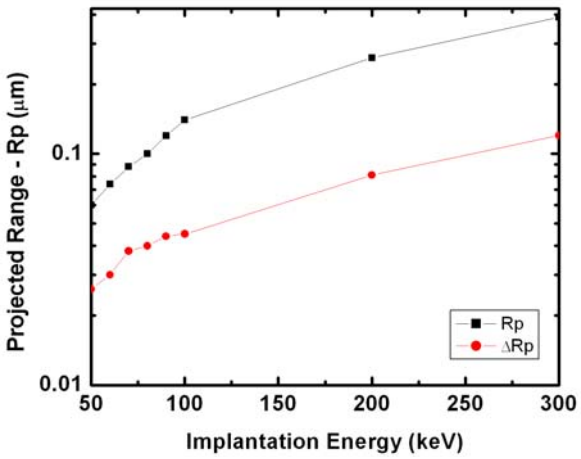


Figure 28. Implantation depth vs. energy of phosphorous into silicon.

An approximation of the necessary implantation dose is calculated with equation (4.32). Where Q is the necessary dose for the peak concentration of the implanted ions to

stop at R_p, and N_p is the desired volumetric concentration after implantation and diffusion. For the thermal cantilevers the desired volumetric concentration, N_p, has two values, 1e17 atoms/cm^3 for the heater region, and 1e20 atoms/cm^3 for the legs. Based off of these numbers Q_{htr} = 2.25e12 atoms/cm^2 and Q_{leg} = 2.25e15 atoms/cm^2 respectively.

$$Q = \sqrt{2\pi}\, N_p\, \Delta R_p \tag{4.32}$$

Further refinement of the dose specification is done with Ssuprem3 which simulates the diffusion process and outputs a volumetric concentration vs. depth profile. Using this software and the original implantation dose is refined along with determining the diffusion parameters. For this study the refined implantation dose for the heater and leg regions were $Q_{htr,\ avg}$ = 5.61e12 atoms/cm^2 and $Q_{leg,\ avg}$ = 5.61e15 atoms/cm^2 respectively.

4.2.2 Diffusion Simulation with Ssuprem3

Ssuprem3 determined the diffusion parameters, temperature and time, necessary to spread and active the implanted phosphorous. Post implantation the ions are closely packed at a specific distance (R_p) below the top surface of the silicon device, see Figure 29. A diffusion step spreads the ions throughout the cantilever thickness. Ideally the ions evenly diffuse throughout the implanted volume, but this is not the case. Ssuprem3, though, simulates the implantation and diffusion and outputs volumetric concentration and diffusion depth information. By inputting the dopant material and implantation parameters such as energy, tilt angle, and dose a closer approximation of the impurity distribution is established. An example Ssuprem3 input file is given in Appendix C. Using this method the optimal dose and diffusion parameters are determined.

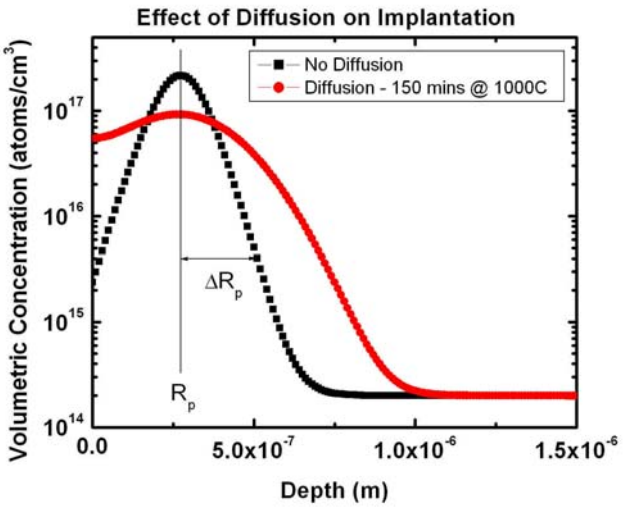


Figure 29. Effect of diffusion on implantation.

Ssuprem3 simulations show that post the initial low dose implantation a diffusion time of 30 minutes at a temperature of 1000°C diffuses the phosphorous dopants a minimal 3700Å into the cantilever thickness. Because there still remains a high dose implantation step for the legs and anchor, which includes another diffusion step, only part of the total diffusion for the low dose implantation is completed. The diffusion rate between the low and high dose implantations is different and depends upon the implanted impurity concentration. Higher concentration implantations diffuse faster into silicon when compared to lower concentration implantations. Therefore two diffusion steps are necessary to fully active the entire thickness of silicon in the heater region.

Heating the cantilevers to 1000°C for 120 minutes post high dose implantation diffuses the dopants in the leg and anchor more than 1.5μm. Under these conditions the dopants in the heater region diffuse and additional 1300Å, for a total diffusion length of approximately 5000Å. Figure 30 shows the phosphorus ion diffusion in the heater and anchor regions.

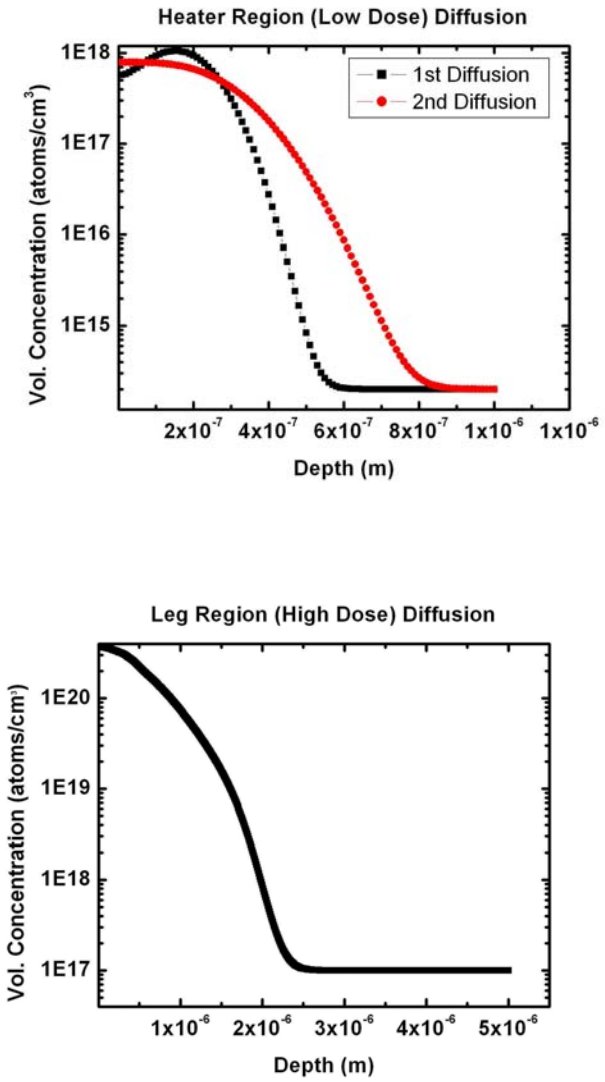


Figure 30. Distribution of phosphorous in the heater and leg region of the thermal cantilever.

CHAPTER V

EXPERIMENTAL RESULTS

Chapter V describes the experimental characterization of the fabricated heated AFM cantilevers. A deep understanding of the cantilever electrical and thermal characteristics is essential to applying this tool to metrology and surface modification applications. The measurements described in this chapter seek to develop a calibration technique that allows the end user to know exactly what the cantilever response will be for a given input.

Three experimental techniques were used to determine different cantilever characteristics. Electrical measurements were taken with industry standard equipment to determine the heated AFM cantilever electrical properties, while Raman spectroscopy was used to measure the cantilever thermal response. By using the cantilever to measure the known topography of a sample, estimates of the approximate tip shape were determined.

Only steady state electrical and thermal measurements were taken. The chapter is divided into sections that describe the electrical measurements, temperature measurements, and imaging resolution.

5.1 Experimental Electrical Measurements

It is important to understand what inputs to the heated AFM cantilever lead to specific thermal, resistive, and power outputs. To test a cantilever a Keithley 2400 source-meter, which is in series with the cantilever and sense resistor, supplies the circuit

with varying voltages. In parallel, across the sense resistor, an Agilent 34401A 6 ½ digit multi-meter measures the sense resistor voltage. Electrical Signatone probes contact the aluminum leads on the bulk silicon of the cantilever and provide the electrical contact to the heated AFM cantilever. Figure 31 diagrams this circuit.

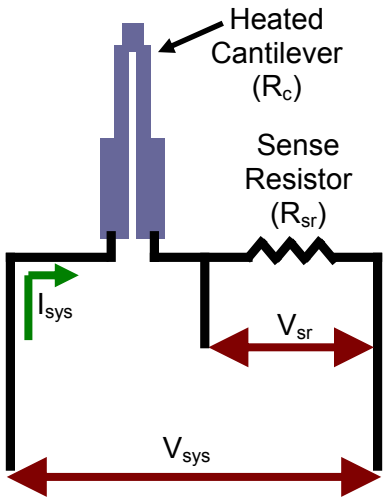


Figure 31. Circuit for characterizing a heated AFM cantilever electrical properties.

In this configuration the voltage applied to the circuit and sense resistor are read using the source-meter and multi-meter respectively. Applying Ohm's law to the known sense resistor, the system current can be calculated (5.1).

$$I_{sys} = \frac{V_{sr}}{R_{sr}} \tag{5.1}$$

The voltage across the cantilever is also known since it is the difference in the total applied current and the current across the sense resistor (5.2).

$$V_c = V_{sys} - V_{sr} \tag{5.2}$$

Ohm's law is applied again and the cantilever resistance calculated (5.3).

$$R_c = \frac{V_c}{I_{sys}} \tag{5.3}$$

Seventeen cantilevers of each type (A – F) were chosen at random from a wafer, imaged in an SEM and electrically tested as described above. Resulting cantilever thickness measurements were approximated from SEM images and the results listed in Table 4.

Table 4. Cantilever thickness measurements made in SEM.

Cantilever	**Thickness (μm)**	**Cantilever**	**Thickness (μm)**	**Cantilever**	**Thickness (μm)**
A1	1.35	B1	1.0	C1	1.05
A2	0.8	B2	1.25	C2	1.0
A3	0.9	---	---	C3	0.7
D1	1.3	E1	1.25	F1	1.05
D2	0.8	E2	0.5	F2	1.3
D3	1.15	E3	1.25	F3	1.5

Individual cantilevers were tested in air with the backside of the cantilever approximately 550μm away from the nearest surface. The sense resistor was approximately 1000Ω, and the system input voltage was varied from 0.2 to 10V in steps of 0.2V. Results from cantilevers A and E are shown in Figure 32 and Figure 33. Other cantilevers exhibited similar results and are given in Appendix D.

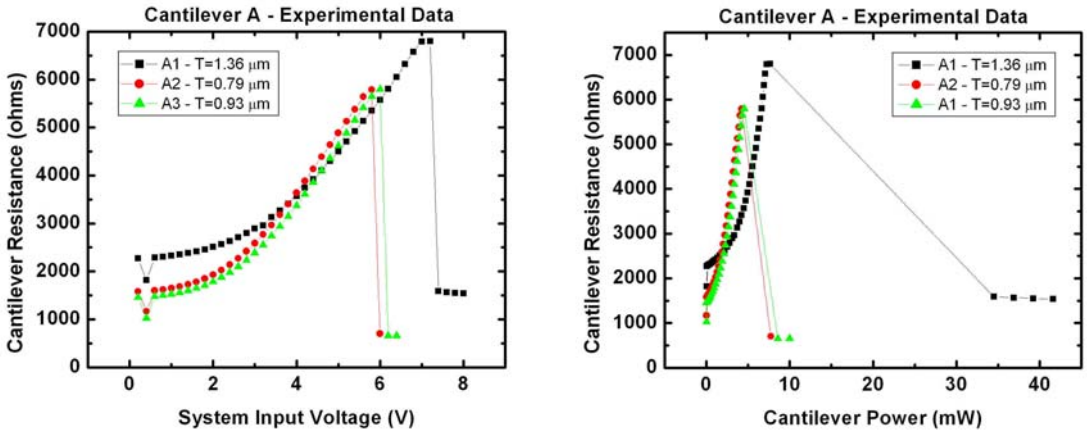


Figure 32. Measured cantilever electrical resistance and power of cantilever A.

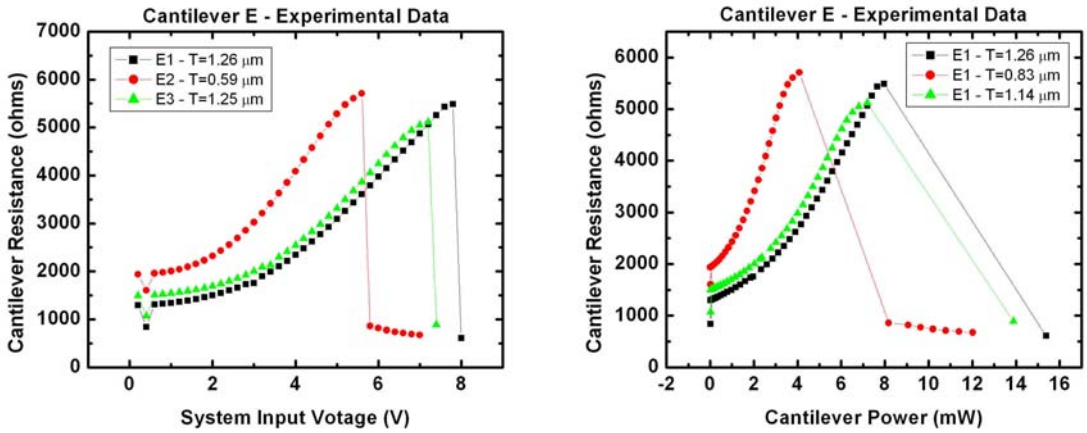


Figure 33. Measured cantilever electrical resistance and power of cantilever E.

Figure 32 and Figure 33 show the cantilever resistance climbing as the system input voltage increases, but dropping to a value below the starting resistance at a specific voltage. Similar trends describe the cantilever resistance vs. cantilever power figures. Cantilever resistance climbs with increasing power and then drops. The drop in

resistance, even with increasing power, is attributed to thermal runaway which is a characteristic of semi conducting materials.

Thermal runaway depends upon temperature, material and doping concentration. At a specific temperature the intrinsic carrier concentration of doped silicon exceeds the dopant carrier concentration. When this occurs the electrical resistance of the material decreases and is governed by the intrinsic carrier density rather than the doping concentration. The decrease in resistivity, due to the extra carriers that become available, increases the current flow though the material. An increase in current generates more resistive heating that increases the temperature which further drops the resistance. This positive feedback loop continues until the device burns out or is restricted by a current limiting element.

Figure 34 shows the resistivity vs. temperature dependence of the cantilever heater and leg regions. Equations (4.24) and (4.25) model this relationship [21]. The thermal runaway effect in the heater region can be interpreted as the downward slope of the heater curve and begins when the heater temperature reaches the turnover point in this curve. The phosphorous density in the cantilever leg region is 3 orders of magnitude larger than the phosphorous density in the heater. Thus, the heater region reaches the critical temperature for thermal runaway before the leg region.

Due to the smaller number of carriers available in the heater region, the thermal runaway effect is only an issue for this region. As the system input voltage increases so does the heater temperature. When the heater temperature reaches a specific value, or critical temperature, its resistance begins to drop. The value at which this occurs is the turnover temperature on the temperature/resistivity curve for a specific volumetric

concentration of impurities. At temperatures above the critical temperature the resistivity drops which drops the heater resistance. The continual increase in temperature, though, increases the mobility of the impurities in the silicon which allows more current to travel though the cantilever thus increasing the power.

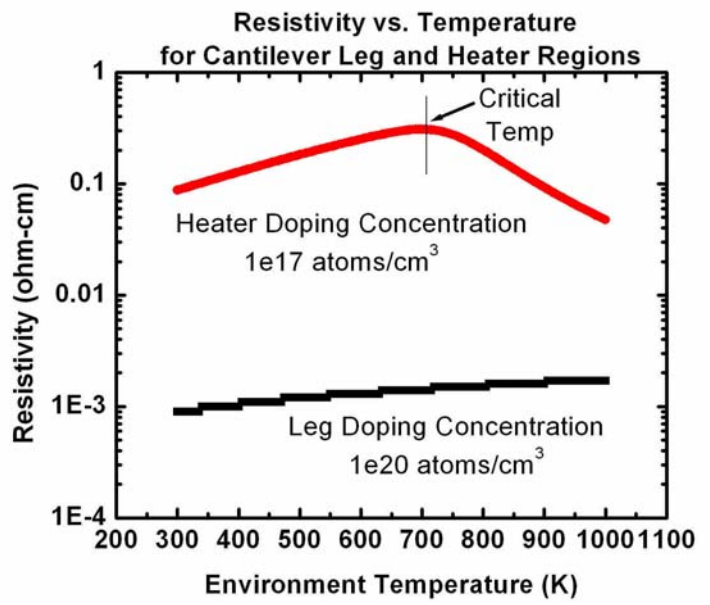


Figure 34. Resistivity vs. temperature relationship.

Figure 34 not only shows the effects of thermal runaway, it also shows that the resistivity of the heater is at least 3 orders of magnitude larger than the resistivity of the legs. The average heater doping concentration is approximately 1e17 atoms/cm^3, while the average leg concentration is 1e20 atoms/cm^3. Heater resistivity and resistance values are consistently 2 orders of magnitude larger than the leg resistivity values.

5.2 Temperature Measurements Using Raman Spectroscopy

Raman spectroscopy is a common technique that uses the characteristic atomic vibrations of a compound to identify a substance. Recently Raman spectroscopy has been applied to the thermal analysis of non-metallic surfaces with temperature sensing capabilities ranging from room temperature to over 1000°C and spatial resolution of less than 1μm [23].

The Raman system focuses a laser on a surface and collects a small portion, 1 in 10^7, of the elastically and inelastically scattered photons. The system filters much of the elastic component (Rayligh) and uses the inelastic component (Stokes) for determining specific material properties. Vibrational states within the crystal lattice create differences in the energy between the incident light and the scattered photons through the creation or annihilation of phonons. This inelastic scattering creates longer (Stokes shift) or shorter (Anti-Stokes shift) wavelength measurements which appear in the Raman spectra as shifted peaks. These peaks, or frequency shifts, produce a signature which is temperature, stress, and/or crystal structure dependent. It has been shown that stress and crystal structure may have a smaller effect on the Raman signature when compared to temperature effects for some materials [24]. Thus, material specific calibrations of Stokes shift with temperature allows for temperature measurements of other devices of the same material to be easily computed. However, the effect of stress is geometry dependent and should be investigated with changes in sample geometry.

To apply this temperature characterization method to heated AFM cantilever characterization requires that the Raman system be calibrated with materials that closely resemble the cantilever material. When the grain size of polysilicon is greater than

100nm Raman spectroscopy does not distinguish between polysilicon and single crystal silicon. Thus, calibration of the Raman system was done with three samples of phosphorous doped polysilicon that had been annealed at 1100°C to ensure large grain size. One sample was implanted at 4e20 atoms/cm^3 to imitate the cantilever legs, while the other two samples were implanted to 4e16 and 4e18 atoms/cm^3 to imitate the heater region. Post implantation each sample was diffused for 60 minutes at 1100°C. Calibration was also done on undoped polysilicon and single crystal silicon for comparison purposes.

During testing a Linkam TS1500 environment controlled hot stage varies the stage temperature from 100°C to 1000°C in steps of 100°C. At each temperature the Raman system collects a Raman signature and correlates it to the known stage temperature. To properly simulate the heater region, the results from the two samples of polysilicon were averaged inducing only a +/- 2°C error.

Two heated AFM cantilevers were chosen for two different Raman measurement techniques. The first technique measures only the Stokes peak to calculate temperature, but this technique is influenced by stress within the device. To remove the stress effects completely, a second technique was used that utilizes the ratio of the Stokes and Anti-Stokes peak intensities for temperature measurements. This is valid since the ratio fo the two peaks depends on the available phonon states which is given by the Bose-Einstein distribution function, which is dependent upon temperature and not stress.

To test the cantilever it was put into series with a sense resistor of 10kΩ, and an input voltage was applied across the pair. This is the same circuit as described throughout various sections of this study with a 10kΩ resistor in place of a 1kΩ resistor.

The input voltage was varied from 0V to 14V in steps of 0.5V. Raman signatures were collected at 6 different locations along the cantilever heater, thermal constriction and leg. Comparison with the previous calibration signatures at specific temperatures allowed for the temperature calculation of each point along the cantilever. Figure 35 shows the locations of the 6 temperature measurements.

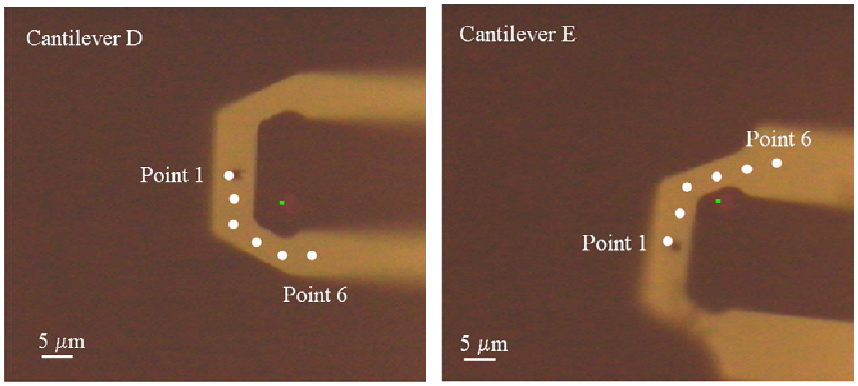


Figure 35. Raman system image of cantilevers D & E. Locations of temperature measurements are indicated by the white dots.

Figure 36 and Figure 37 A and B graph the experimental temperature, electrical resistance, and system input voltage cantilever *D* data taken for the 6 data points for the Stokes and Stokes/Anti-Stokes methods respectively. Each of the data points exhibit similar trends. There is an exponential increase in cantilever temperature with respect to system input voltage and an approximate linear increase in temperature with respect to cantilever power.

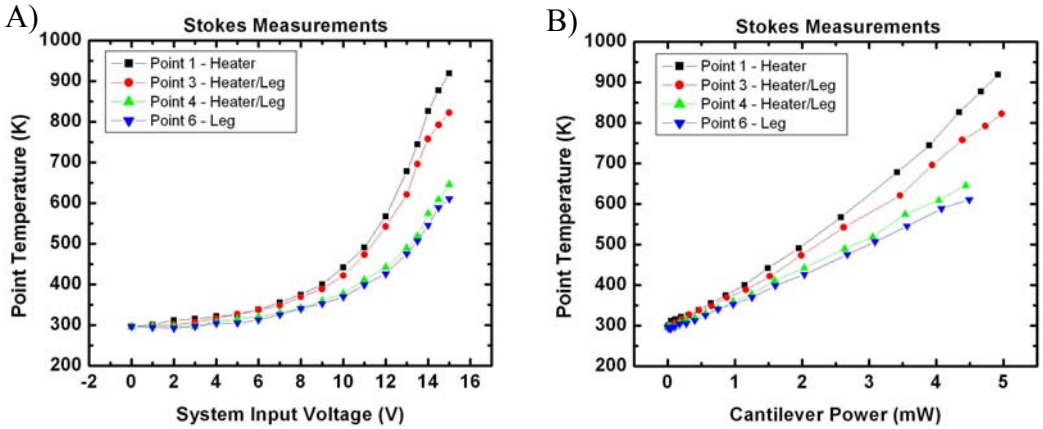


Figure 36. Raman Stokes measurements. A) Point temperature vs. the system input voltage. B) Point temperature vs. cantilever power.

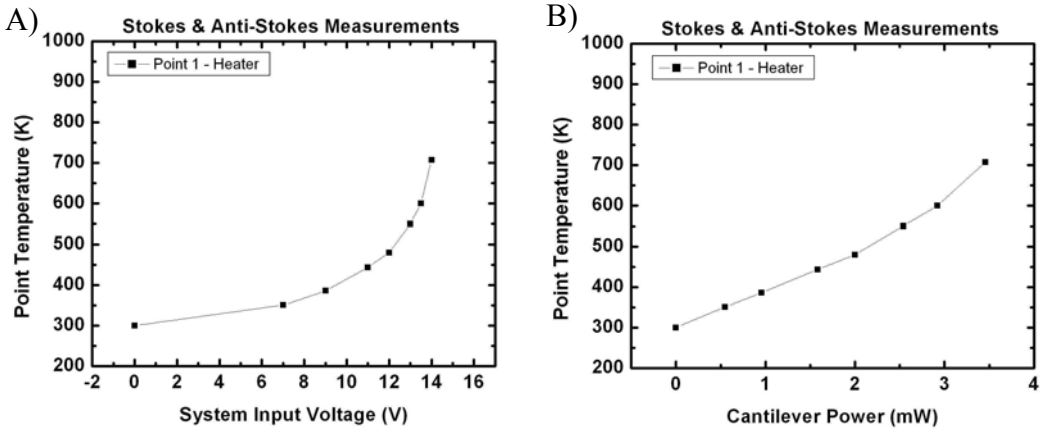


Figure 37. Raman Stokes and Anti-Stokes measurements. A) Point temperature vs. the system input voltage. B) Point temperature vs. cantilever power.

Note that the hottest point on the cantilever was identified as the point directly above the heater. The other measured points were progressively cooler as the measurement location was moved away from the heater.

Figure 38 is a comparison of the Stokes and Stokes/Anti-Stokes measurement techniques. As the figure shows, the two techniques produce similar measurements, but may begin to diverge at higher cantilever power inputs. The divergence of the two

techniques can be attributed to lack of system calibration at higher temperatures. This comparison, though, demonstrates one of two things; in using only the Stokes measurements to calculate cantilever temperature the stress can be considered negligible, or the cantilever is stress free since both techniques closely match. Other studies with the heated AFM cantilever suggest that the device bends upon heating which induces a stress in the cantilever. This shows that using only the Stokes peaks for temperature measurements is acceptable and that the stress free cantilever scenario can be considered incorrect.

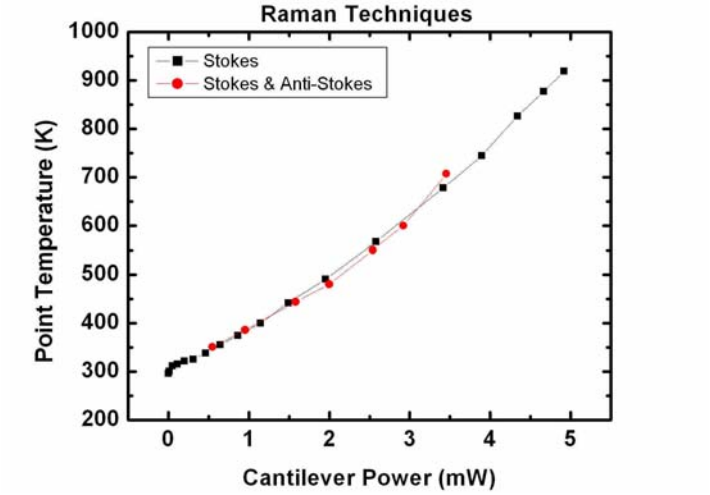


Figure 38. Comparison of Stokes and Anti-Stokes measurements, heater point.

5.3 Resolution Based on Tip Radius

One factor in determining the imaging resolution of AFM cantilevers is the overall tip height and radius of curvature. It is advantages to have a tall slender tip such that it will follow the surface topography even when the surface has narrow and deep crevices. The tip must also be durable and should not bend or break under the loading

conditions necessary for imaging. Commercially available cantilevers have a standard tip radius of curvature on the order of 30nm, while special tips can be found with a radius of curvature under 10nm (Park Scientific Instruments). The cantilevers fabricated for this study all had an approximate tip height of 1μm as determined by SEM micrographs, see Figure 39 for reference, and an approximate tip radius of curvature of 20nm.

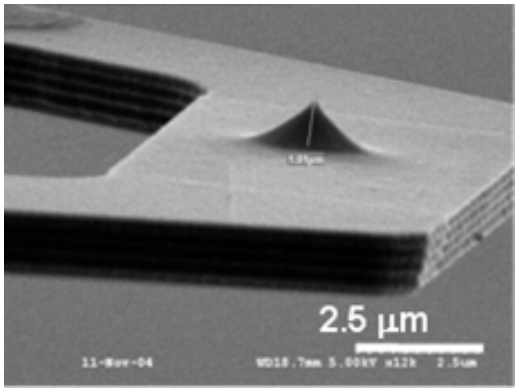


Figure 39. SEM images of a heated AFM cantilever tip. Tip height = 1.01μm.

The heated AFM cantilever tip radius of curvature approximation was done by imaging a surface of known dimension. An un-powered heated AFM cantilever was attached to a commercially available AFM head and scanned over an indium surface. Structures of known size exist on the surface and were imaged. The resulting scans showed resolution near 20nm thus approximating the tip radius to be at or below that value. Figure 40 shows the results of a surface topography scan using a heated AFM cantilever.

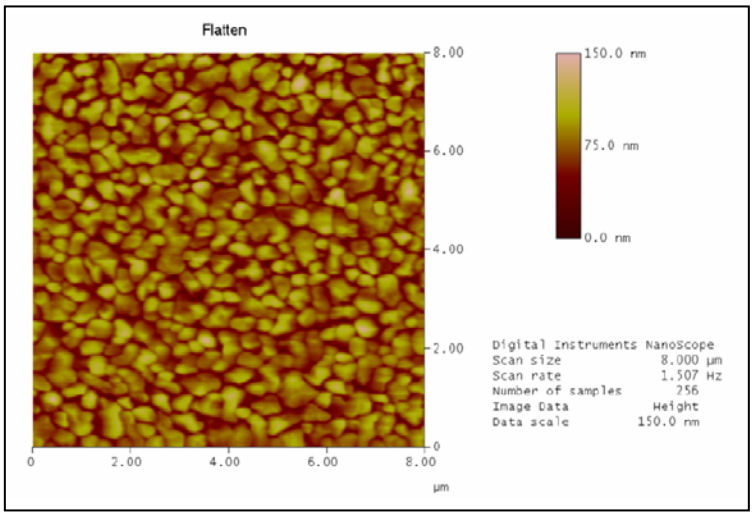


Figure 40. Heated AFM cantilever image of indium. Resolution is estimated to be better than 20nm.

CHAPTER VI

THEORETICAL RESULTS & COMPARISONS WITH EXPERIMENTAL DATA

For many applications of heated AFM cantilevers it is essential to have a characterization or calibration method. Part of the characterization is understanding the relationship between the heated AFM cantilever system inputs and outputs. This chapter focuses on the results from the theoretical model, as described in Chapter IV, and compares these results against the experimental data discussed in Chapter V.

6.1 Theoretical Results

Predictions from the theoretical model qualitatively compared with the experimental results. Simulations made predictions for every experiment and in the upcoming sections the resulting resistance vs. system input voltage and power vs. system input voltage predictions will be discussed. Theoretical temperature trends along the length of the cantilever, the effects of varying cantilever geometry and a discussion of the dominating heat transfer coefficients also follow.

To save on computation time without sacrificing accuracy, all theoretical computations use a control volume increment size of 0.5μm. A brief study on the effect of control volume size showed only small changes in node temperature, approximately 0.1K, or cantilever resistance, approximately 1Ω, as the size was varied from 0.1, 0.25, 0.5 to 1μm.

6.1.1 Theoretical Electrical Results

Cantilever thicknesses and variable doping profile, for both the heater and leg regions, were necessary for each simulation. Table 4 lists the approximate individual cantilever thicknesses, as determined by SEM imaging. Ssuprem3 diffusion software provided the variable doping profile for each cantilever. The final doping profile through the cantilever thickness is not the same for every cantilever. The buried oxide layer is a reflective boundary condition for the diffusing phosphorous ions. Because each cantilever varies in thickness, thinner cantilevers are affected by the oxide layer while thicker cantilevers are not.

Only the results of cantilever *A* are shown in Figure 41, but the theoretical power and system input voltage vs. resistance results of the remaining cantilevers are given in Appendix E. The theoretical results shown here display the same trends exhibited by the experimental results. Cantilever resistance increases with both power and system input voltage, but drops drastically at a specific input voltage or power input. This abrupt change in resistance is attributed to the thermal runaway effect, i.e. the temperature dependent resistivity of the silicon, which was discussed in Chapter V.

For both experiment and simulations the thickest cantilever, A1, had the lowest overall resistance and reached its maximum electrical resistance at a higher voltage than the thinner cantilevers. This result makes sense since the cantilever resistance is inversely proportional to the cross-sectional area of the cantilever, and thinner cantilevers have a smaller cross-section.

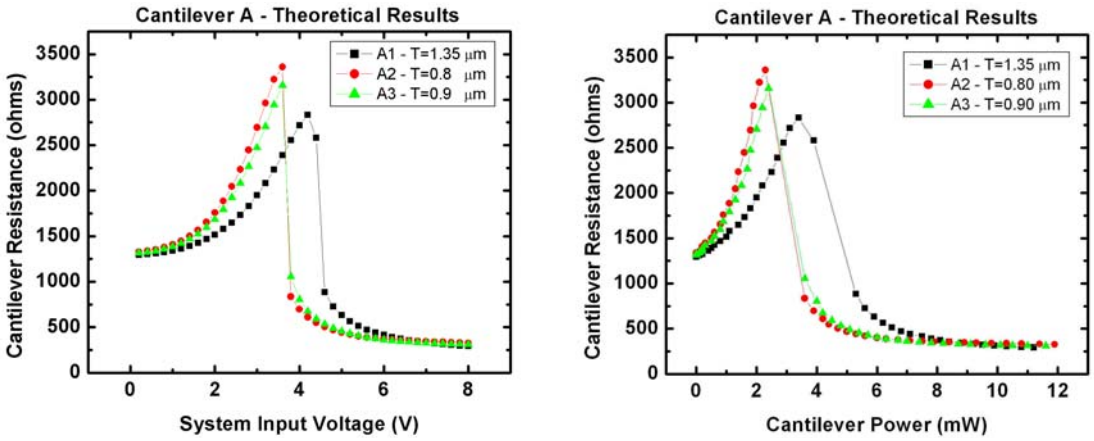


Figure 41. Theoretical resistance and power results for cantilever *A*.

6.1.2 Theoretical Temperature Results

Figure 42 shows the cantilever tip temperature response vs. system input voltage for cantilever *A2*. The system input voltage was increased from 0.25V to 6V in steps of 0.25V, and the tip node temperature recorded. As expected the tip temperature increases with increasing voltage, although there is a discontinuity at approximately 4V. At voltages above 4V the thermal runaway effect drives the resistance lower, which generates more heater power, which drives up the heater temperature. This positive cycle continues and the temperature increases until the heater eventually burns out.

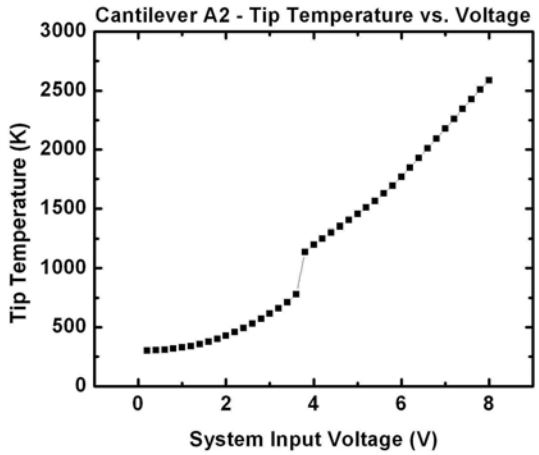


Figure 42. Cantilever *A2* tip temperature increases until the thermal runaway effect occurs and creates a jump in the curve.

Figure 43 shows the node temperature along cantilever *A2* for varying voltages. As expected the overall cantilever temperature increases with increasing voltage. The cantilever-anchor connection always has a temperature at or near 300K. This result is expected since a 300K boundary condition exists to the left of the first node.

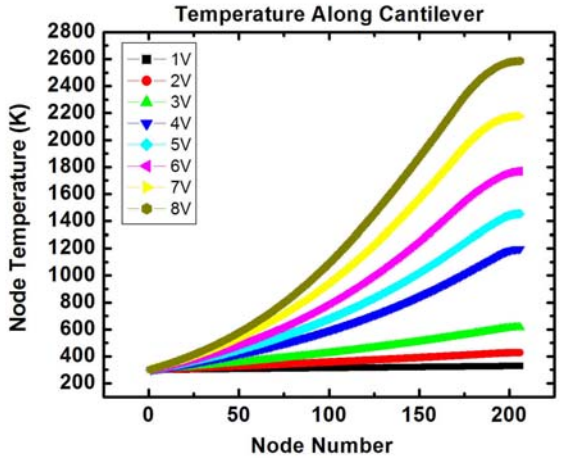


Figure 43. Cantilever *A2* - theoretical cantilever temperature distribution as a function of system input voltage.

The temperature distribution along the length of the cantilever starts at the base silicon temperature and then increases until the temperature levels off in the last 10 nodes. This leveling effect corresponds to the heater region which encompasses the last 10 nodes within the cantilever model.

Another phenomenon to note is the difference in the temperature distribution below 3V and above 4V. In the 1 to 3V range the temperature distribution shows a linear distribution along the cantilever length. At low voltages, and in this test configuration for which the cantilever is in air and not near a surface, the system heat transfer is dominated by the heat conduction from the heater into the legs. The presence of another heat transfer mode would remove the linearity. At 4V and above the linear temperature distribution disappears because the heat cannot conduct from the heater to the legs fast enough. The obstruction of heat creates a warmer heater region and a non-linear temperature distribution along the cantilever legs.

6.1.3 Effect of Geometry on Theoretical Results

The 6 cantilevers designed for this study, A – F, all geometrically vary from one another. Using the theoretical model it was possible to determine what effect changes in geometry have on the cantilever thermal and electrical response. Two simple scenarios were run for cantilever *A2*. In the first scenario the leg width is changed from 5 to 10 to 15μm, while in the second scenario the leg length was changed from 50 to 85 to 135μm. Figure 44 shows the cantilever resistance vs. input voltage curves for both scenarios.

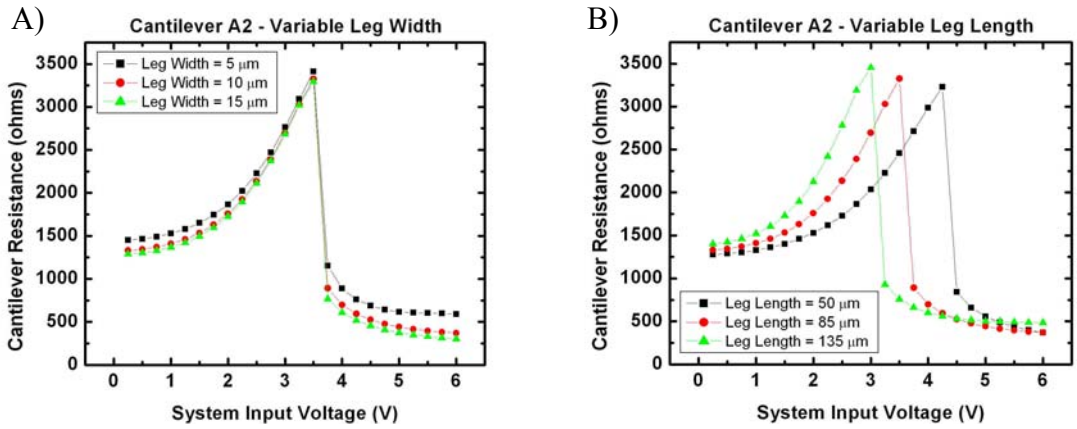


Figure 44. Cantilever *A2* theoretical resistance as a function of system input voltage. A) Variable leg width. B) Variable leg length.

Varying leg width has little effect on the final cantilever resistance but does impact the cantilever resistance at the lower and upper end of the system input voltages. The opposite is true of the cantilever length. Varying the cantilever length changes the maximum resistance obtained and the system input voltage at which the maximum occurs. A longer cantilever theoretically has a lower maximum resistance and achieves this resistance at a higher voltage when compared to a shorter cantilever.

The higher maximum resistance achieved by the shorter cantilever could be attributed to the bulk silicon at the base of the anchor, which acts as a sink for the heat generated. Therefore with a shorter cantilever more heat is delivered from the cantilever legs to the bulk silicon thus reducing the cantilever temperature.

6.1.4 Dominating Heat Transfer Coefficients

To determine the dominating heat transfer effects a simplified theoretical simulation was created that modeled the 4 heat transfer modes of the cantilever: conduction through the gap to the surface below the cantilever, convection to the environment, radiation to the environment, and conduction through the cantilever. This

basic model sets each node to a specified temperature rather than using electrical system inputs and material properties to calculate the temperature. All calculations used the heat transfer coefficients given in Table 2.

Simulation results showed that when the cantilever is infinitely far from any surface the heat conducted through the cantilever legs is at least 4 orders of magnitude larger than any other heat transfer coefficient. At these distances the other heat transfer forms can be neglected. Table 5 summarizes the magnitude of each heat transfer coefficient when the cantilever is near a surface. The conduction through the gap to the substrate becomes large enough, within 1 order of magnitude when compared to the conduction through the cantilever legs, at smaller gap distances to have an effect on the resulting cantilever temperature. Therefore at smaller gap distances the conduction through the gap cannot be neglected.

Table 5. Relative heat transfer coefficient values (W) when the cantilever is near a surface.

Heat Transfer Coefficient	**Gap = 0.5 μm**
Conduction through the Gap	10^{-5}
Convection to the Environment	10^{-10}
Radiation to the Environment	10^{-7}
Conduction through Cantilever Legs	10^{-4}

Figure 45 shows the normalized heat conductances as a function of node temperature and further reinforces that when the cantilever is near a surface the conduction from the cantilever to the surface below adds to the resulting heat transfer effects. The convection and radiation to the environment experience little to no change

whether the cantilever is close to or far from another surface and therefore may be neglected in both cases.

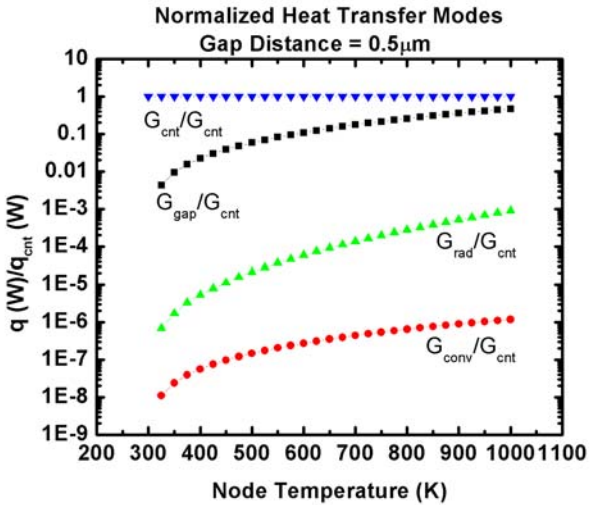


Figure 45. Normalized heat transfer modes between thermal cantilever and surface/environment.

6.2 Experimental vs. Theoretical Results

The experimental electrical response of the cantilever was compared against the theoretical electrical output from the model, while the experimental thermal response of the cantilever, as indicated by Raman spectroscopy, was compared against the temperature predictions. Cantilever *A2* is used unless otherwise stated.

6.2.1 Electrical Response

Figure 46 shows the experimental and theoretical electrical responses from cantilever *A2*. The resistance and power trends are the same, but differ in value. In Figure 46A both cantilevers start out within 500Ω of one another and climb in resistance at approximately the same rate. The two sets of data deviate when the theoretical

resistance drops at approximately 4V while the experimental data continues to climb until nearly 6V. Similar trends are applicable to the power vs. system input voltage curves.

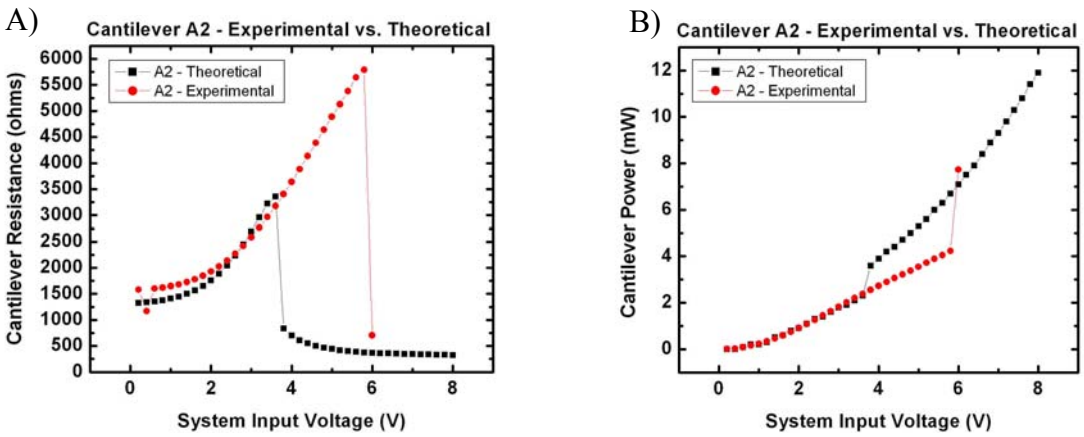


Figure 46. Cantilever *A2* experimental and theoretical electrical results.

Two theoretical investigations, heater geometry and resistivity, examined the discrepancy between the theoretical and experimental results. The influence of other variables was neglected since many variables are predetermined, such as the emissivity of silicon and the thermal conductivity of air, and can be found in literature.

6.2.1.1 Heater Geometry

During diffusion the implanted phosphorous ions diffuse both vertically and horizontally. As is, the theoretical model assumes that the dopants only diffuse into the cantilever thickness and do not spread horizontally. To account for this type of impurity movement, the heater size should be decreased.

Ssuprem3 simulations estimate that for the diffusion temperature and time used during fabrication the impurities diffuse approximately 2μm into the silicon. If the assumption is made that the impurities move the same distance laterally, then the heater

length could be reduced by as much as 4μm. Three simulations were run that varied the heater length for cantilever *A2* from the original 10μm to 8μm and finally 6μm. Figure 47 shows the results of these simulations.

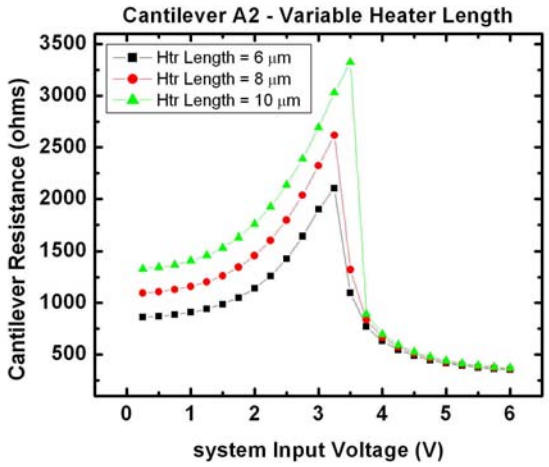


Figure 47. Cantilever *A2* theoretical results from varying the heater length.

Heater length has a considerable impact on the cantilever resistance at voltages below the turnover in the resistance vs. voltage curve. As the heater length decreases, so does the cantilever resistance which is expected since the majority of the cantilever's resistance comes from the heater region. The horizontal phosphorous diffusion though has the opposite impact on cantilever resistance, when discussing the discrepancy in the theoretical model and experimental data. Heater size was ruled out as a potential cause of the low theoretical resistance values.

6.2.1.2 Variable vs. Constant Volumetric Doping Concentration

The next study compared a variable and constant volumetric doping concentration through the cantilever thickness. Previous research used a constant volumetric concentration through the cantilever thickness [18], while Ssuprem3 simulations showed

that post implantation and diffusion the volumetric concentration of ions was actually variable. Theoretical simulations were run for these two cases. The first case explored a variable volumetric concentration. Diffusion time and temperature values used during heated cantilever fabrication, along with cantilever thickness, were inputs for Ssuprem3. The generated variable volumetric concentration numbers for cantilever *A2* were subbed into the theoretical code. The second case used a constant volumetric concentration of 3.12e17 atoms/cm^3 in the heater region. This number is the average of the variable volumetric concentration data generated by Ssuprem3 for the first case.

Figure 48 graphs the results of this investigation. Both the variable and constant volumetric concentrations do not correctly represent the experimental data. The constant concentration though does increase the maximum resistance and pushes the turnover voltage to a higher value. This trend of increasing resistance and turnover voltage is positive and therefore the effect of a constant volumetric concentration should be investigated further in future work.

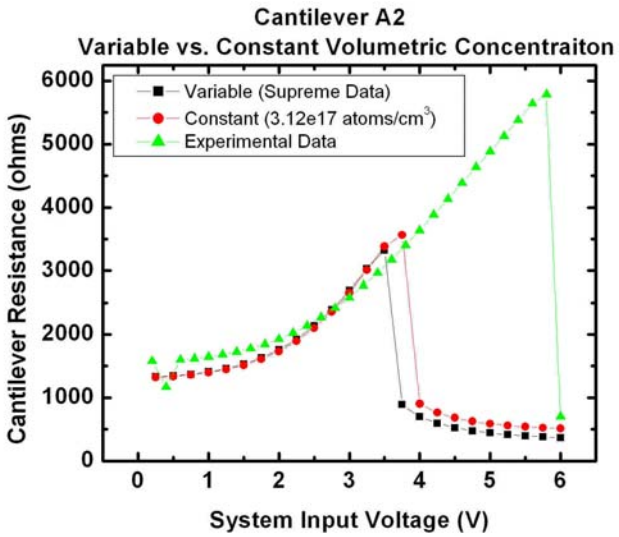


Figure 48. Effect of variable vs. constant volumetric concentration.

6.2.2 Thermal Response

Raman spectroscopy temperature measurements were made of 6 points on 2 different cantilevers, *D* and *E*, for a range of system input voltages. The theoretical model duplicated the experimental set up in that a 10kΩ sense resistor was used along with the specific doping information for the cantilever thickness.

The theory predicted that the hottest spot would be above the tip at the free end of the cantilever and then progressively cool into the thermal constriction and cantilever legs. This trend was exhibited by the tested cantilevers. Temperature trends and values between the experimental Raman data and the theoretical results exhibit very different behavior. Figure 49 shows the graphical results.

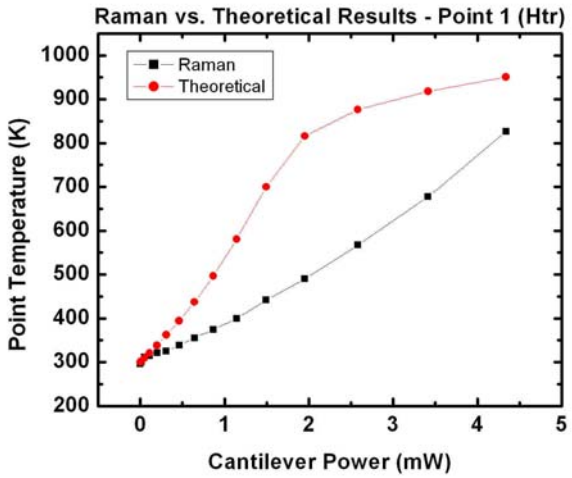


Figure 49. Experimental point temperature using Raman vs. theoretical node temperature of cantilever *D*.

The difference in behavior between the experimental and theoretical data is not fully understood. Similar to the characterization results there are still open questions as

to the effect of the implantation diffusion, cantilever geometry, and applicable heat transfer modes on the theoretical model. These were discussed in the previous section.

CHAPTER VII

CONCLUSION AND FUTURE WORK

7.1 Conclusions

In this study there were 2 main objectives: to fabricate heated AFM cantilevers and to characterize their behavior. Heated AFM cantilevers were successfully fabricated at the Georgia Institute of Technology, making Georgia Tech the third place in the world where these cantilevers have been fabricated, only behind IBM Zurich and Stanford University. The fabrication process and mask sets designed produced 6 different cantilever types of varying geometry. Each fabricated wafer produced more than one hundred working devices. Of the cantilevers tested the average cantilever thickness was 1.07μm. A resolution study with one cantilever indicated that the tip radius of curvature was on the order of 20nm.

To characterize the fabricated cantilevers steady state electrical measurements were performed on 17 devices. The resulting resistance and power vs. input voltage curves behaved in a manner predicted by previous research. At a voltage, specific to the individual device, each cantilever would experience a drop in resistance or a jump in power which was attributed to the thermal runaway effect.

The cantilever temperature response due to an input voltage was also evaluated. Temperature measurements at given system inputs were taken using Raman spectroscopy. This technique proved to be a potential candidate for future cantilever temperature evaluations since its spatial resolution was less than 1μm and when properly calibrated there is only a +/- 2°C error in temperature measurements.

For aid in characterization a theoretical model, which links the cantilever thermal and electrical response through the heat generated term, was developed. Using finite difference methods the cantilever is divided into nodes and an energy balance applied to each node. The system temperatures are initialized and the temperature dependent variables, such as electrical resistivity and thermal conductivity, are evaluated. An iterative numerical method technique solves for the temperature at each node.

The theoretical model mimicked the experimental set up and was only used for steady state measurements, although time elements have been coded into the model for future transient analysis. A finite volume approach was chosen over finite element simulations since the former allowed control of specific heat transfer parameters.

Also incorporated into the model was volumetric vs. depth into the cantilever data generated using Ssuprem3 software. Thickness determined using SEM imaging was input into Ssuprem3 so that variable volumetric doping concentration information can be resolved for individual cantilevers.

Trends exhibited by the theoretical results match the trends in the experimental data, but overall values calculated by the theoretical model do not accurately predict the experimental results. Possible error sources were discussed.

7.2 Suggestions for Future Work

The key suggestion for future work is to match the theoretical model to the experimental data. A better understanding of impurity diffusion could improve the modeling of the device. To increase the heated AFM cantilever model accuracy it is essential that the actual doping concentration versus depth be determined. Four point probe measurements or the introduction of Van der Pauw test structures onto a wafer test

the bulk resistivity of a wafer. The bulk resistivity alone though does not give any information about the volumetric concentration at specific depths.

To find specific impurity profile measurements spreading-resistance or secondary ion mass spectroscopy (SIMS) techniques could be used. Both techniques, though, are destructive. With spreading-resistance measurements a region of the doped device is angle lapped and a 2 point probe measures the resistivity as a function of depth on the lapped surface. From these measurements impurity depth vs. concentration information is obtained.

SIMS is another destructive resistivity measurement technique that uses a low energy ion beam to remove/sputter atoms from the surface 1 or 2 atomic layers at a time. The mass spectrometer collects and analyzes a small percentage of the sputtered atoms producing information about the volumetric concentration vs. depth. The sensitivity of this technique surpasses any of the techniques mentioned previously.

As a recommendation, a combination of these techniques should be integrated into the heated AFM cantilever fabrication process. An area large enough for 4 point probe measurements could be integrated into the mask set, along with creating Vad der Pauw test structures. These two techniques would only give bulk resistivity values. To determine the actual doping profile versus depth spreading-resistance or SIMS measurements could be carried out on test structures. Small samples of silicon that imitate the device material and thickness could be implanted and diffused along with the wafers holding the cantilevers. These small samples could then be used for the destructive spreading-resistance and SIMS characterization measurements.

The cantilevers fabricated and tested all received the same implantation and diffusion treatments. Thus, any issues with the implantation or diffusion affect all cantilevers. More cantilevers should be fabricated that vary the implantation and diffusion. A longer diffusion of the heater region dopants may lead to a more uniform volumetric concentration, which in turn would affect the resulting resistances.

Once the theoretical model and experimental results match the theoretical model can be used as a calibration tool for future fabricated cantilevers.

APPENDIX A

FABRICATION PROCESS DETAILS

Heated AFM Cantilever Beam Process				
Wafer Material				
1	Material	**Material:**	SOI Wafer <100> 5 μm - 1 μm - 550 μm	3.2.1
Measure Silicon Thickess				
2	Tip	**Equipment:**	Nanospec	3.2.1
		Recipe:	Record min thickness	
Oxide Deposition				
3	Tip	**Equipment:**	Unaxis PECVD	3.2.1
		Recipe:	Program Name: LSMSIO2.prc Thickness: 5500 Å Time: 7.5 mins	
Measure Oxide Thickess				
4	Tip	**Equipment:**	Nanospec	3.2.1
		Recipe:		
Shipley 1813				
5	Tip	**Equipment:**	Spinner	3.2.1
		Recipe:	HMDS Primer - 3000/500/15 1813 - 2500/500/33 HP - 115C/5min Thickness = ~1.5 μm	
Photolithography of Mask #1 (2.5 um Tip Structures)				
6	Tip	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.1
		Recipe:	*Exposure* Ch.2 (Wavelength = 405 nm) Lo Vac (20 μm separation) Dose = 112 mJ *Development* MF319 - 1:10 Rinse with DI Water and dry w/ N-gun Resulting PR thickness = ~1.8 μm	
Hard Bake				
7	Tip	**Equipment:**	Hot Plate	3.2.1
		Recipe:	120 °C for 10 mins	
Topside Oxide Etch				
8	Tip	**Equipment:**	Plasma Therm ICP (L)	3.2.1
		Recipe:	Program Name: tlwsio2.bch Etch Depth Needed = 5500 Å Time = 2.5 min	
Topside Silicon Etch (Anisotropic)				
9	Tip	**Equipment:**	STS ICP	3.2.1
		Recipe:	Program Name: m1_tanya.bch Estimated Number of Cycles = 11 Rate = ~0.2 μm/cycle	

Piranha Clean				
10	Tip	**Equipment:**	Wet Bench	3.2.1
		Recipe:	Piranah Solution (H_2SO_4:H_2O_2 :: 70%:30%) Time = 5 min Rinse with DI water and dry with N-gun	
Topside Silicon Etch (Isotropic)				
11	Tip	**Equipment:**	Wet Bench - HNA	3.2.1
		Recipe:	Recipie Used: Etch Depth Needed = 0.5 um HNA - 2% HF, 3% CH_3COOH, 95% HNO_3 Time = ~1.5 min Estimated Etch Rate = ~0.33 μm/min	
Oxidize Wafer (Wet)				
12	Tip	**Equipment:**	Lindberg Furnace #2	3.2.1
		Recipe:	Furnace - 950 °C, 1.5 Hours Bubbler - 70 °C Expected thickness = ~0.34 μm	
Isotropic Silicon Dioxide Wet Etch				
13	Tip	**Equipment:**	Wet Bench	3.2.1
		Recipe:	6:1 BOE Estimated Etch Rate = 1000 Å/min Time = ~4 min	
SEM				
14	Tip	**Equipment:**	SEM	3.2.1
		Recipe:	Measure silicon pillar width	
Oxidize Wafer (Dry)				
15	Tip	**Equipment:**	Lindberg Furnace #2	3.2.1
		Recipe:	Furnace - 950 °C, 5 Hours Expected thickness = ~0.11 μm	
Isotropic Silicon Dioxide Wet Etch				
16	Tip	**Equipment:**	Wet Bench	3.2.1
		Recipe:	6:1 BOE Estimated Etch Rate = 1000 Å/min Time = ~1 min	
SEM				
17	Tip	**Equipment:**	SEM	3.2.1
		Recipe:	Measure silicon pillar width	
Shipley 1827				
18	Cantilever Formation	**Equipment:**	Spinner	3.2.2
		Recipe:	O - 160C/5min 1827 - 3000/1000/35 HP - 115C/3min Thickness = ~2.5 μm	
Softbake/Prebake				
19	Cantilever Formation	**Equipment:**	Hot Plate	3.2.2
		Recipe:	100 °C for 10 mins	

Photolithography of Mask #2 (Beam Structure)				
20	Cantilever Formation	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.2
		Recipe:	*Exposure* Ch.2 (Wavelength = 405 nm) Lo Vac (20 μm separation) Dose = 336 mJ *Development* MF354 - 1:10 Rinse with DI Water and dry w/ N-gun	
Hard Bake				
21	Cantilever Formation	**Equipment:**	Hot Plate	3.2.2
		Recipe:	100 °C for 10 mins	
Topside Oxide Etch				
22	Cantilever Formation	**Equipment:**	Plasma Therm ICP (L)	3.2.2
		Recipe:	*Recipie Used:* tlwsio2a.bch Etch Depth Needed = 1000 A Time = 1 min	
Topside Silicon Etch (Anisotropic)				
23	Cantilever Formation	**Equipment:**	STS ICP	3.2.2
		Recipe:	Program Name: m1_tanya.bch Estimated Number of Cycles = 7 Rate = ~0.2 μm/cycle	
Piranah Clean				
24	Cantilever Formation	**Equipment:**	Wet Bench	3.2.2
		Recipe:	Piranah Solution (H_2SO_4:H_2O_2 :: 70%:30%) Time = 5 min Rinse with DI water and dry with N-gun	
Shipley 1827				
25	Implantation	**Equipment:**	Spinner	3.2.3
		Recipe:	O - 160C/5min 1827 - 3000/1000/35 HP - 115C/3min Thickness = ~2.5 μm	
Softbake/Prebake				
26	Implantation	**Equipment:**	Hot Plate	3.2.3
		Recipe:	100 °C for 10 mins	
Photolithography of Mask #3 (Low Dose Implantation)				
27	Implantation	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.3
		Recipe:	*Exposure* Ch.2 (Wavelength = 405 nm) Lo Vac (20 μm separation) Dose = 336 mJ *Development* MF354 - 1:10 Rinse with DI Water and dry w/ N-gun	

Hard Bake				
28	Implantation	**Equipment:**	Hot Plate	3.2.3
		Recipe:	110 °C for 30 mins	
Ion Implantation of Entire Beam				
29	Implantation	**Equipment:**	Outside Vendor - Core Systems, CA	3.2.3
		Recipe:	2.51e13 atoms/cm^2 / 200 keV / Phosporous	
Piranah Clean				
30	Implantation	**Equipment:**	Wet Bench	3.2.3
		Recipe:	Piranah Solution (H_2SO_4:H_2O_2 :: 70%:30%) Time = 5 min Rinse with DI water and dry with N-gun	
Oxide Deposition				
31	Implantation	**Equipment:**	Unaxis PECVD	3.2.3
		Recipe:	Program Name: LSMSIO2.prc Thickness: 1780 Å Time: 2.5 mins	
Diffusion				
32	Implantation	**Equipment:**	Lindberg Furnace #2	3.2.3
		Recipe:	Furnace - 1000 °C, 0.5 Hours No oxygen in tube	
BOE				
33	Implantation	**Equipment:**	Wet Bench	3.2.3
		Recipe:	6:1 BOE Estimated Etch Rate = 1000 Å/min Time = ~2.5 min	
Shipley 1827				
34	Implantation	**Equipment:**	Spinner	3.2.3
		Recipe:	O - 160C/5min 1827 - 3000/1000/35 HP - 115C/3min Thickness = ~2.5 μm	
Softbake/Prebake				
35	Implantation	**Equipment:**	Hot Plate	3.2.3
		Recipe:	100 °C for 10 mins	
Photolithography of Mask #4 (High Dose Implantation)				
36	Implantation	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.3
		Recipe:	*Exposure* Ch.2 (Wavelength = 405 nm) Lo Vac (20 μm separation) Dose = 336 mJ *Development* MF354 - 1:10 Rinse with DI Water and dry w/ N-gun	
Hard Bake				
37	Implantation	**Equipment:**	Hot Plate	3.2.3
		Recipe:	110 °C for 30 mins	
Ion Implantation of Heater Region				
38	Implantation	**Equipment:**	Outside Vendor - Core Systems, CA	3.2.3
		Recipe:	2.51e16 atoms/cm^2 / 200 keV / 45° tilt / Phosporous	
Piranah Clean				
39	Implantation	**Equipment:**	Wet Bench	3.2.3
		Recipe:	Piranah Solution (H_2SO_4:H_2O_2 :: 70%:30%) Time = 30+ min Rinse with DI water and dry with N-gun	

Asher				
40	Implantation	**Equipment:**	Asher	3.2.3
		Recipe:	Program Name: #1 Time: 3 min	
Oxide Deposition				
41	Implantation	**Equipment:**	Unaxis PECVD	3.2.3
		Recipe:	Program Name: LSMSIO2.prc Thickness: 1780 Å Time: 2.5 mins	
Diffusion				
42	Implantation	**Equipment:**	Lindberg Furnace #2	3.2.3
		Recipe:	Temperature = 1000 C Time = 2 hr	
Shipley 1827				
43	Contact/ Metal Lift Off	**Equipment:**	Spinner	3.2.4
		Recipe:	O - 160C/5min 1827 - 3000/1000/35 HP - 115C/3min Thickness = ~2.5 μm	
Softbake/Prebake				
44	Contact/ Metal Lift Off	**Equipment:**	Hot Plate	3.2.4
		Recipe:	115 °C for 5 mins	
Photolithography of Mask #5 (Open Vias for Metal Contact)				
45	Contact/ Metal Lift Off	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.4
		Recipe:	*Exposure* Ch.2 (Wavelength = 405 nm Hard Contact (20 μm separation) Dose = 340 mJ *Development* MF354 - 1:10 Rinse with DI Water and dry w/ N-gun	
Hard Bake				
46	Contact/ Metal Lift Off	**Equipment:**	Hot Plate	3.2.4
		Recipe:	115 °C for 10 mins	
Topside Oxide Etch				
47	Contact/ Metal Lift Off	**Equipment:**	Plasma Therm ICP (L)	3.2.4
		Recipe:	*Recipie Used:* tlwsio2a.bch Etch Depth Needed = 1000 A Time = 2 min	
Piranah Clean				
48	Contact/ Metal Lift Off	**Equipment:**	Wet Bench	3.2.4
		Recipe:	Piranah Solution (H_2SO_4:H_2O_2 :: 70%:30%) Time = 5 min Rinse with DI water and dry with N-gun	

Futurrex NR7-1500P				
49	Contact/ Metal Lift Off	**Equipment:**	Spinner	3.2.4
		Recipe:	1000/800/40 Thickness = ~2.75 μm	
Soft Bake				
50	Contact/ Metal Lift Off	**Equipment:**	Hot Plate	3.2.4
		Recipe:	150 °C for 1 mins	
Photolithography of Mask #6 (Metal Connections)				
51	Contact/ Metal Lift Off	**Equipment:**	Karl Suss MA-6 Mask Aligner	3.2.4
		Recipe:	*Exposure* Ch.1 (Wavelength = 365nm) Hard (25 μm of separation) Dose = 300 mJ *Pre-Development Bake* Hot Plate, 100C for 1.5 minutes 5 minute cool *Development* RD6 for 20 sec Rinse with DI Water and dry w/ N-gun	
BOE				
52	Contact/ Metal Lift Off	**Equipment:**	Wet Bench	3.2.4
		Recipe:	6:1 BOE Estimated Etch Rate = 1000 Å/min Time = 20 sec	
Topside Aluminum Deposition				
53	Contact/ Metal Lift Off	**Equipment:**	E-Beam Evaporator	3.2.4
		Recipe:	*Recipie Used:* 7000 Å Aluminum 3 Å/sec	
Liftoff - Acetone Soak to Remove PR/Metal Layer				
54	Contact/ Metal Lift Off	**Equipment:**	Wet Bench	3.2.4
		Recipe:	RR2 Resist Stripper 80° C Time = 20 min	
Sintering				
55	Implantation	**Equipment:**	Lindberg Furnace #3	3.2.3
		Recipe:	Temperature = 400 C Time = 0.5 hr	
Apply Thick Photoresist (PR) to Topside				
56	Release	**Equipment:**	Spinner	3.2.5
		Recipe:	Create protective layer AZ 4620 1500/750/35 Thickness = ~ 13.5 μm	
Hard Bake				
57	Release	**Equipment:**	Hot Plate	3.2.5
		Recipe:	115 °C for 5 mins	

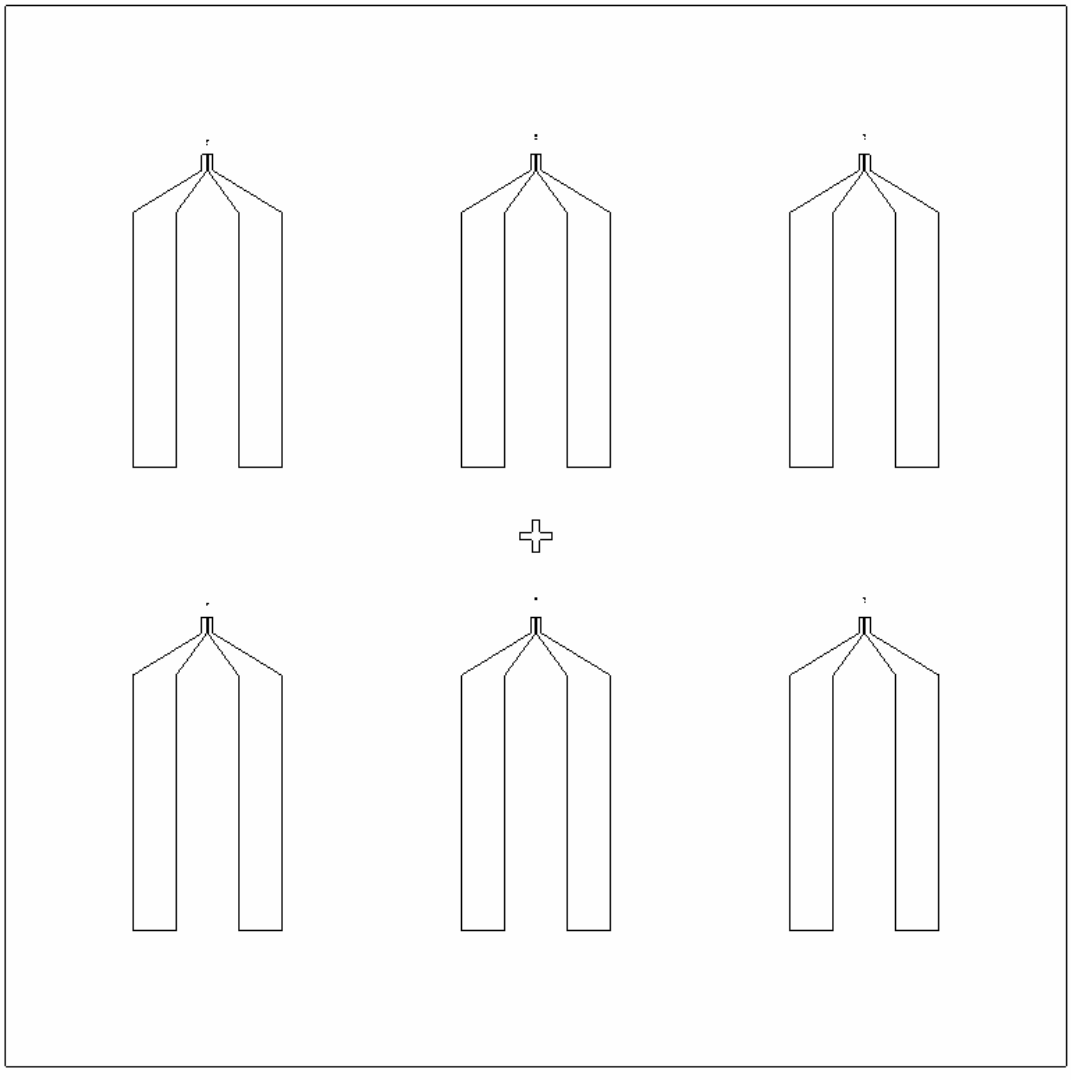
Apply Thick Photoresist (PR) to Bottomside				
58	Release	**Equipment:**	Spinner	3.2.5
		Recipe:	Create protective layer AZ 4620 1500/750/35 Thickness = ~ 13.5 μm	
Softbake/Prebake				
59	Release	**Equipment:**	Hot Plate	3.2.5
		Recipe:	115 °C for 5 mins	
Photolithography of Mask #7 (Backside Openings)				
60	Release	**Equipment:**	EVG Mask Aligner	3.2.5
		Recipe:	*Exposure* Hard Contact (25um of separation) Time = 40 sec Dose = 300 mJ/cm2 *Development* AZ400K:DI, 1:2 for 1 min Rinse with DI Water and dry w/ N-gun	
Hard Bake				
61	Release	**Equipment:**	Hot Plate	3.2.5
		Recipe:	110 °C for 10 mins	
Cleave Wafer				
62	Release	**Equipment:**	Work Bench	3.2.5
		Recipe:	Cleave wafer into 4 quadrants	
Apply Thick Photoresist (PR) to Topside of Carrier Wafer				
63	Release	**Equipment:**	Spinner	3.2.5
		Recipe:	Create protective layer AZ 4620 1500/750/35 Thickness = ~ 13.5 μm	
Attach 1/4 Wafer to Carrier Wafer				
64	Release	**Equipment:**	By Hand	3.2.5
		Recipe:	N/A	
Hard Bake				
65	Release	**Equipment:**	Hot Plate	3.2.5
		Recipe:	110 °C for 15 mins	
Backside Oxide Etch				
66	Release	**Equipment:**	Plasma Therm ICP (L)	3.2.5
		Recipe:	Program Name: tlwsio2.bch Time = 2 min	
Backside Silicon Etch				
67	Release	**Equipment:**	Plasma Therm ICP (R)	3.2.5
		Recipe:	Program Name: twsifsta.bch Estimated Number of Cycles = 1500	
Soak to Separate Wafers				
68	Release	**Equipment:**	Wet Bench	3.2.5
		Recipe:	Photoresist Stripper AZ400T Time = overnight	
HF Release				
69	Release	**Equipment:**	Wet Bench	3.2.5
		Recipe:	HF 49% Thickness = 1 μm Time = 30 sec Dry on a hot plate	
SEM				
70	Release	**Equipment:**	Hitachi SEM	3.2.5
		Recipe:	N/A	

*** *Updated 4/6/05*

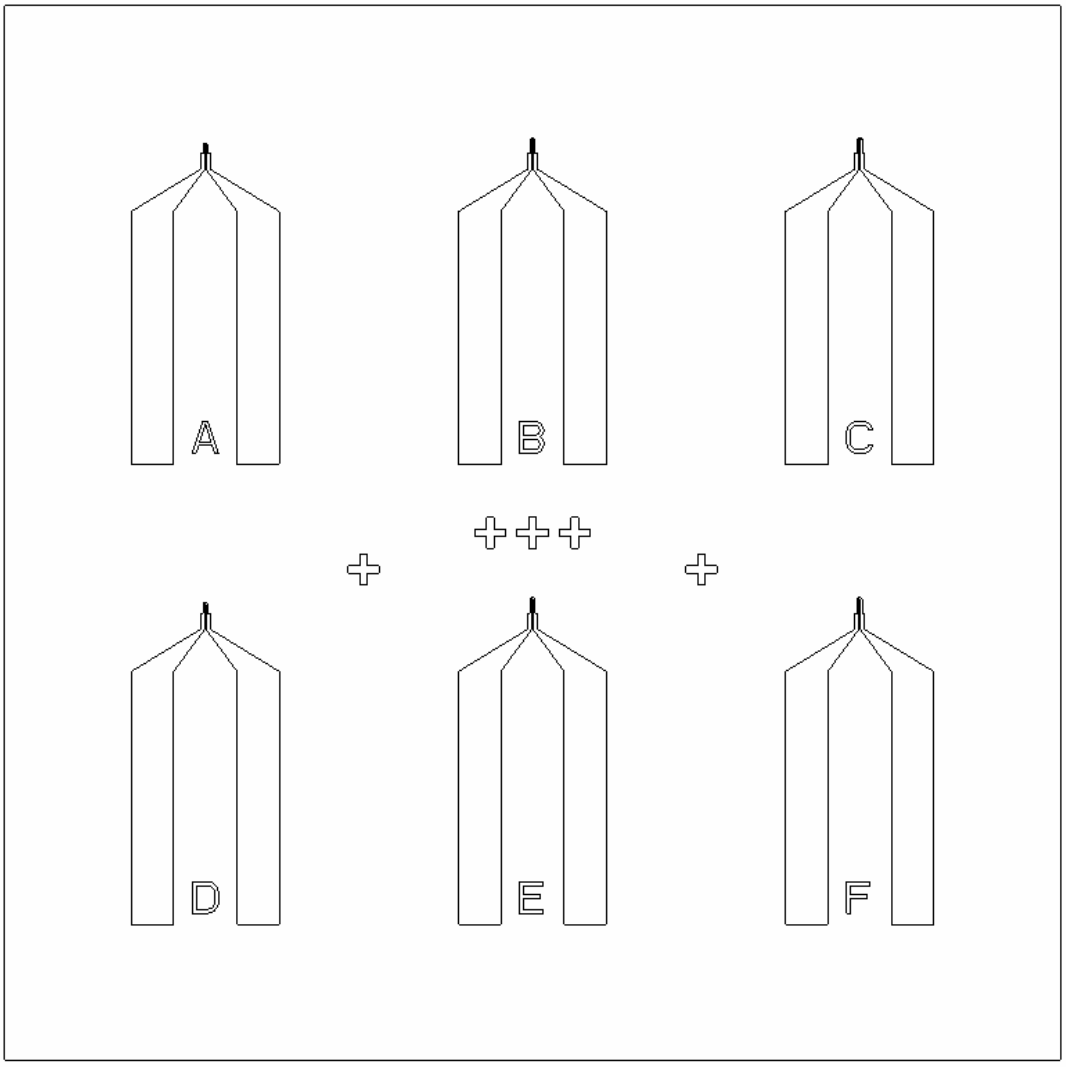
APPENDIX B

MASK DESIGN

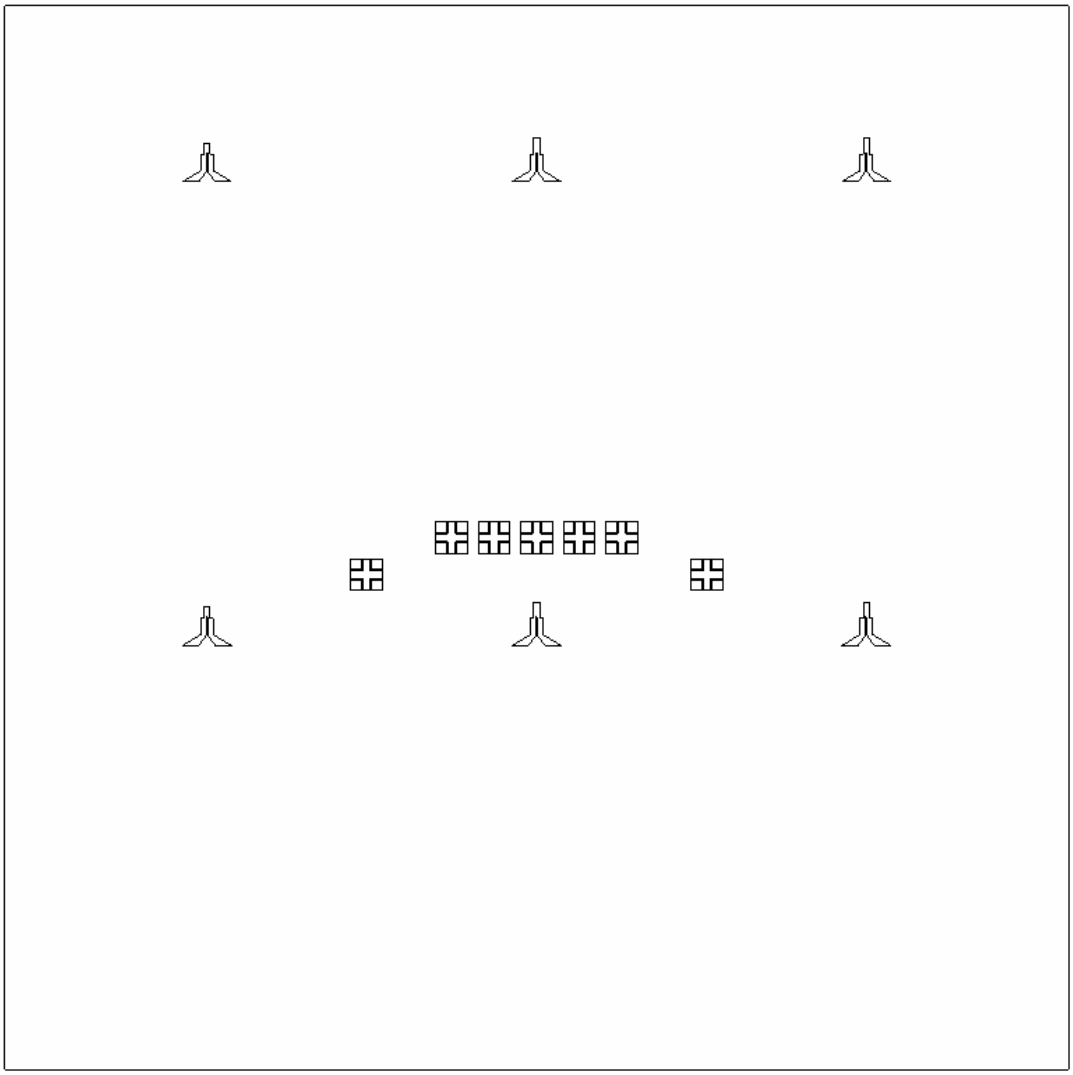
B1. Tip Mask



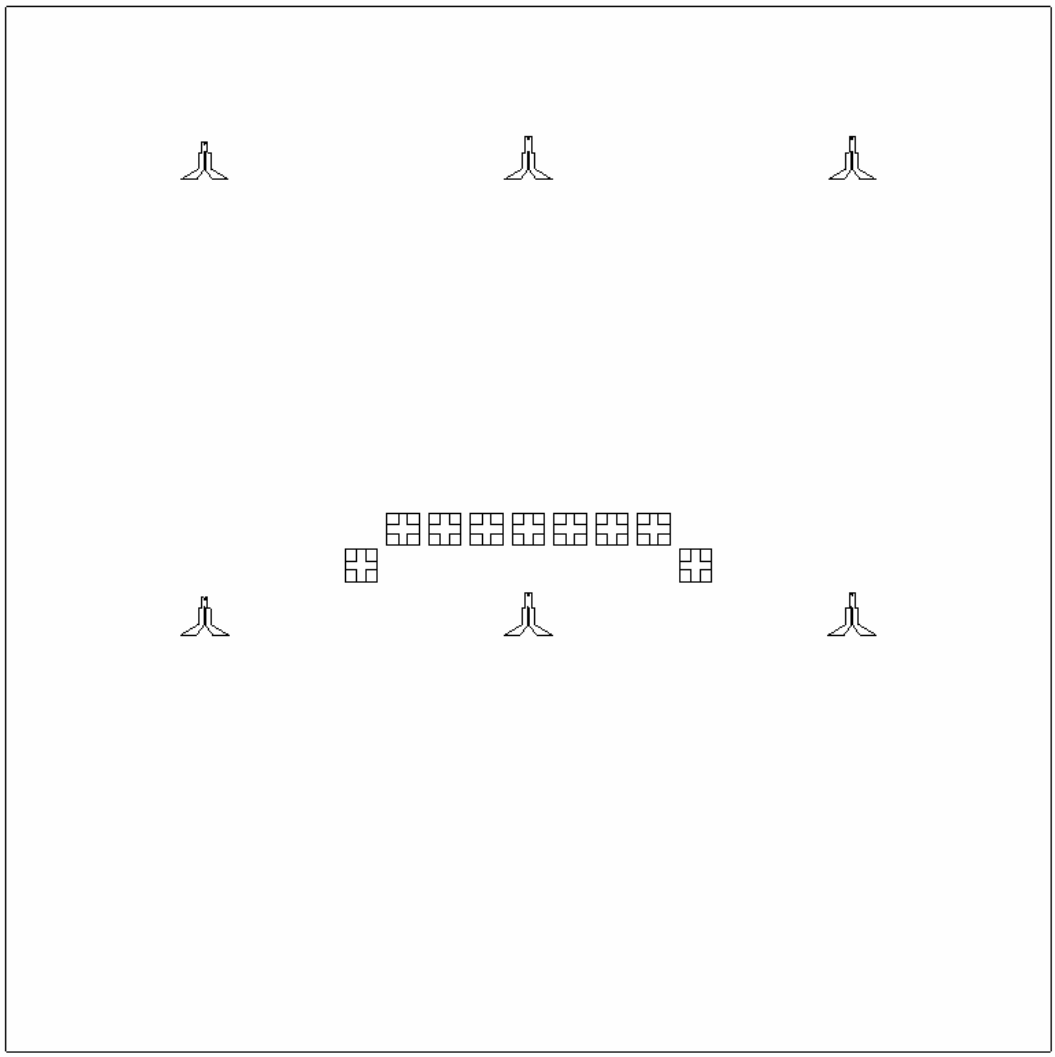
B2. Cantilever Structure Mask



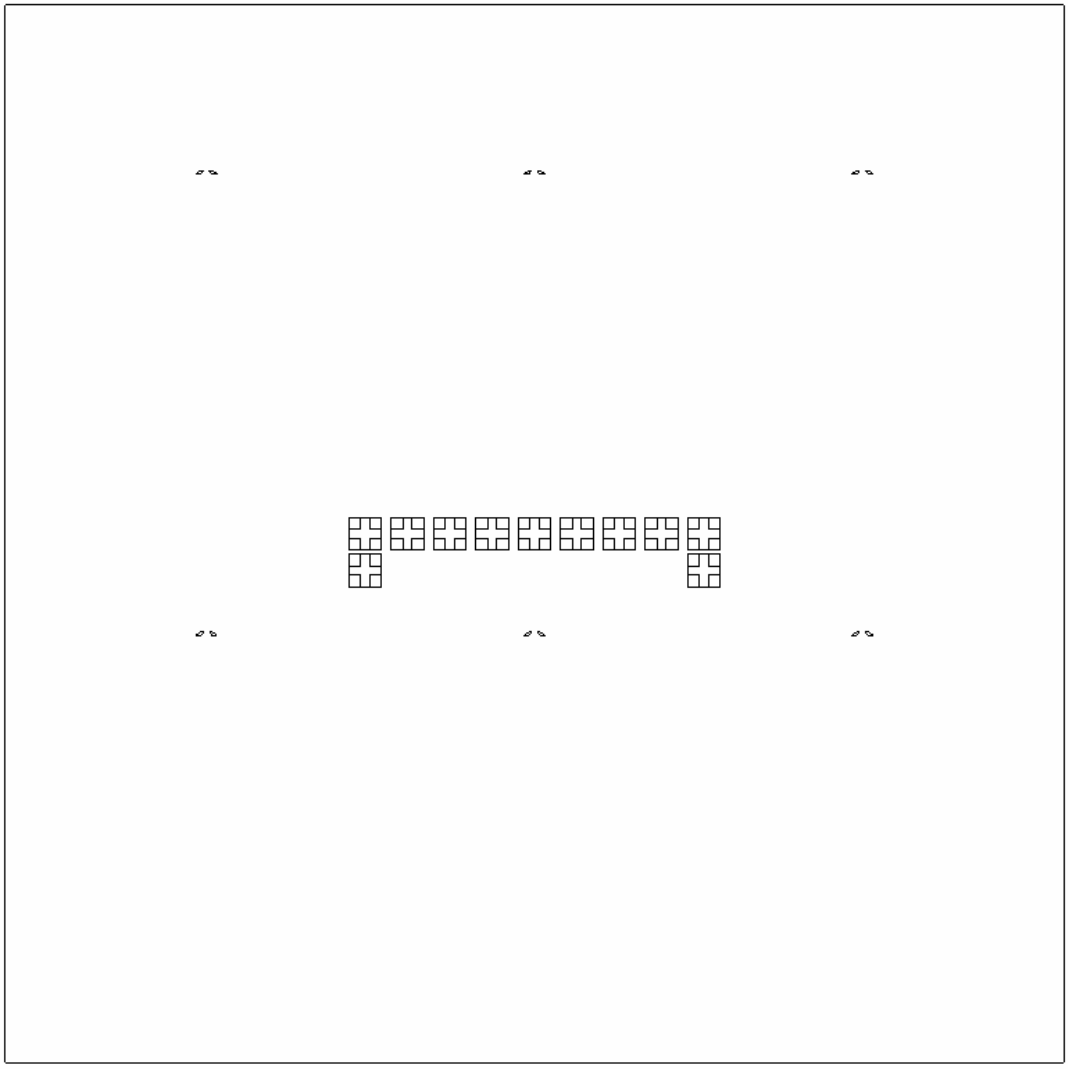
B3. Low Dose Implantation



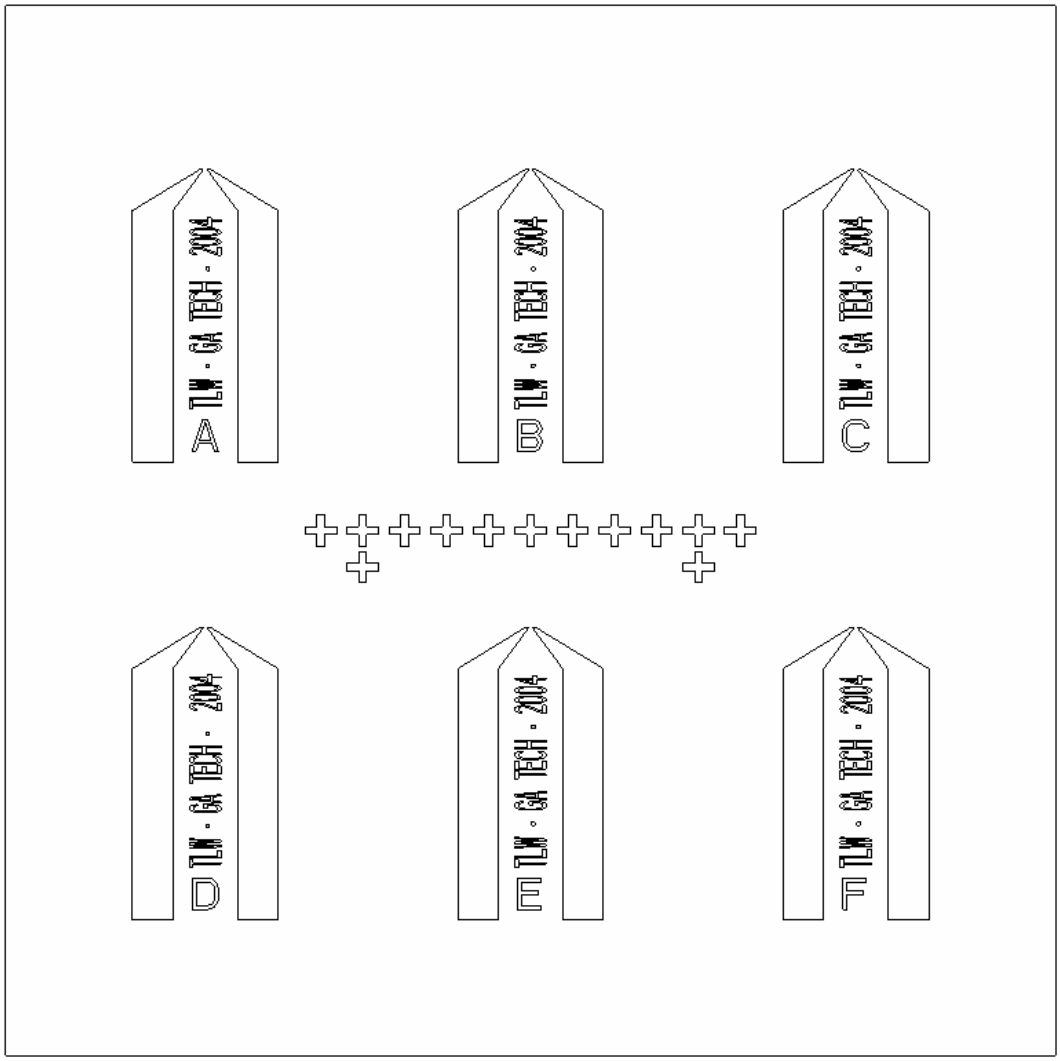
B4. High Dose Implantation



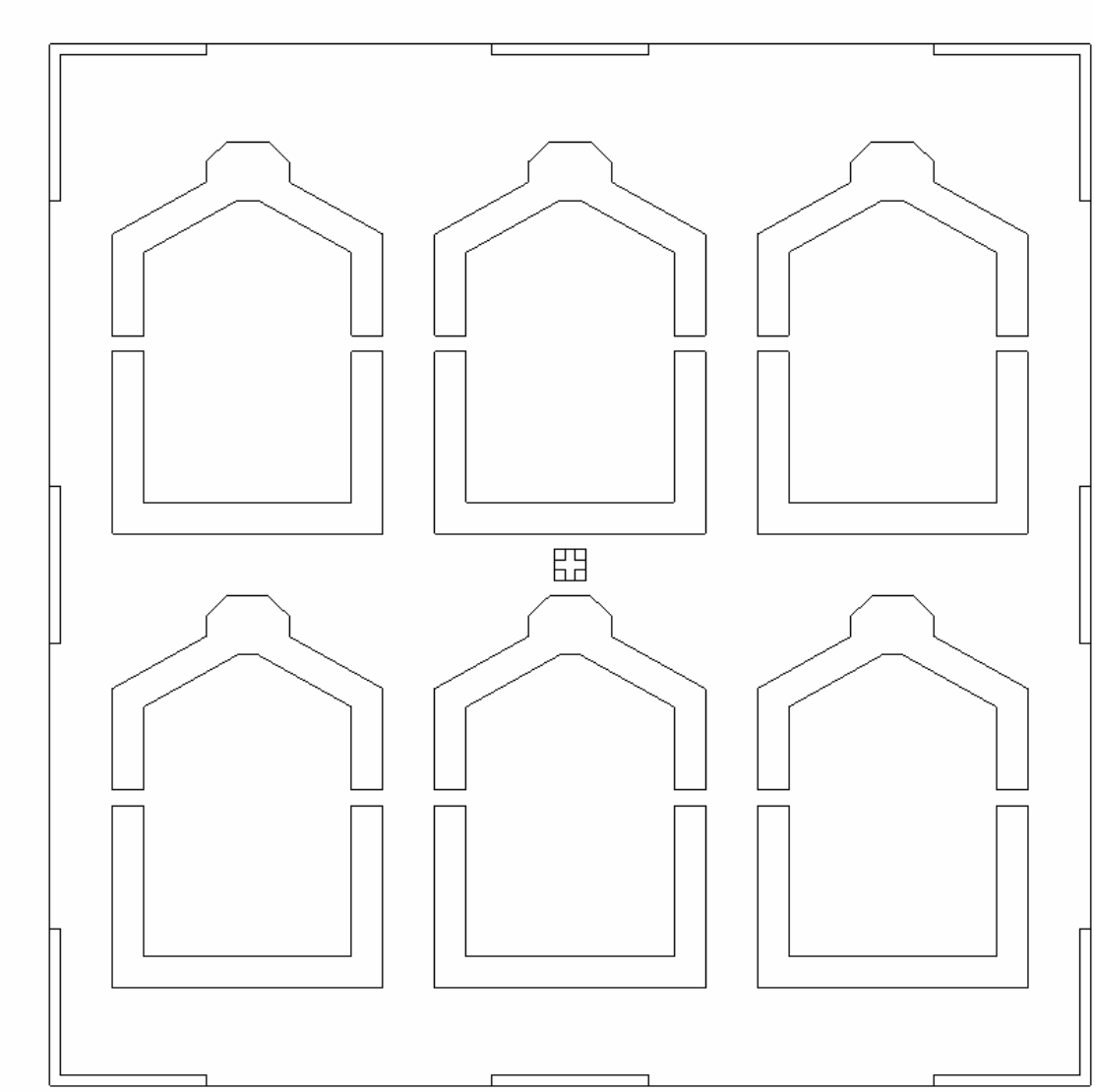
B5. Contacts



B6. Lift Off


A TLW - GA TECH - 2004
B TLW - GA TECH - 2004
C TLW - GA TECH - 2004
D TLW - GA TECH - 2004
E TLW - GA TECH - 2004
F TLW - GA TECH - 2004

B7. Backside Etch



APPENDIX C

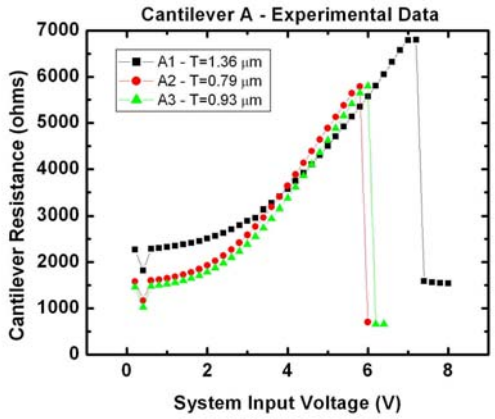
SSUPREME CODE

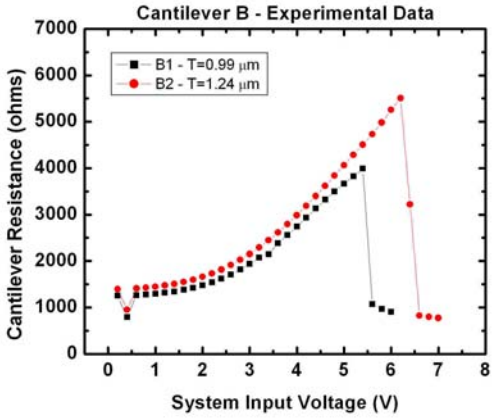
```
go ssuprem3

#comment      base layer
Initialize    <100> silicon c.phosphorous=2e14 \
              thickness=1

#comment      buried oxide layer
Deposition    oxide thickness=1

#comment      device layer
Deposition    <100> silicon c.phosphorous=2e14 \
              thickness=1.5

#comment      Ion Implantation
Implant       Phosphorous dose=4e12 energy=200

#comment      Deposition
Deposition    Oxide Thickness=0.175

#comment      Drive in - Includes the 1st 30 min diffusion
Diffusion     time=150 temperature=1000

#comment      Remove Oxide
Etch          Oxide all

structure     outfile=1_27_soi_ld_150_15.str

structure outfile=1_27_soi_ld_150_15.txt
```

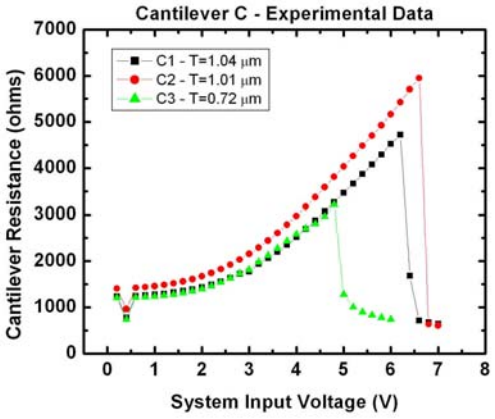
APPENDIX D

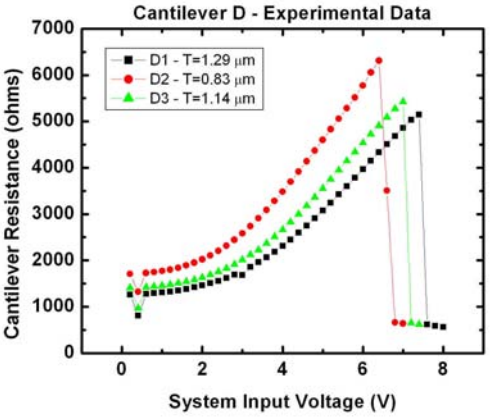
EXPERIMENTAL DATA

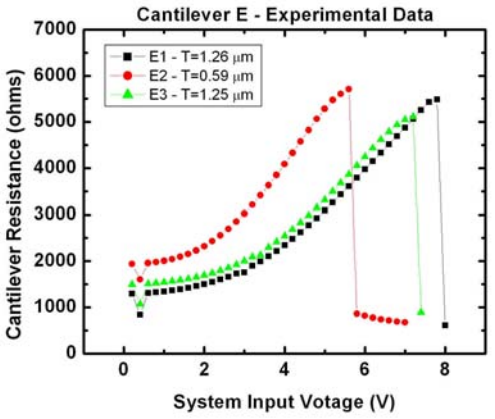
D1. Cantilever Resistance vs. System Input Voltage

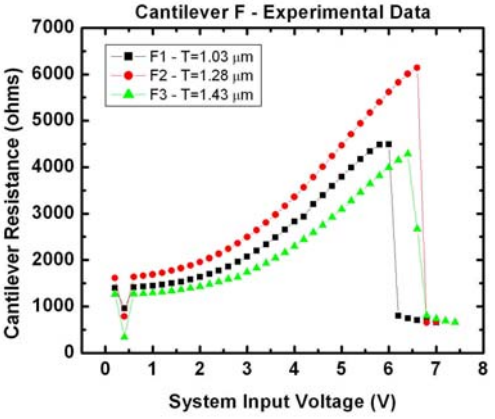




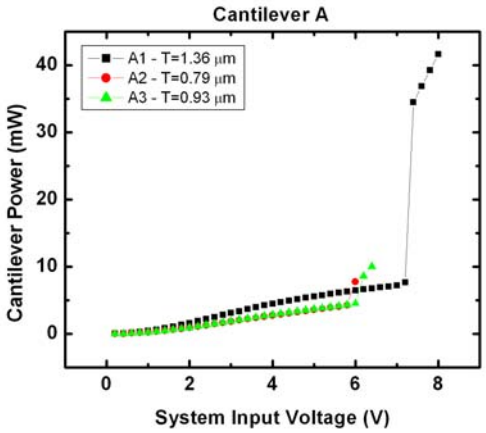


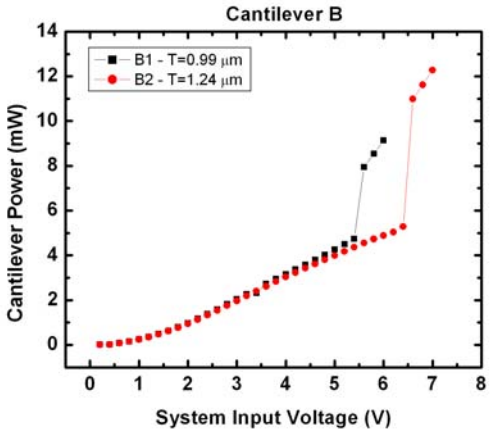


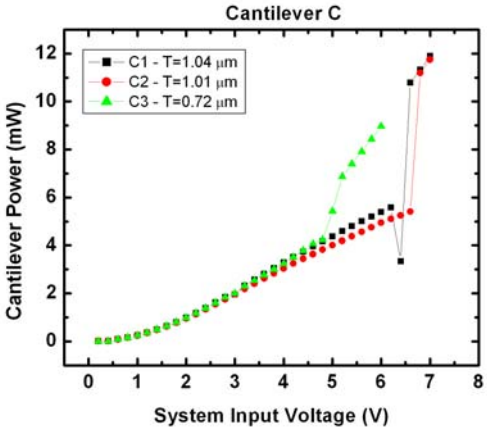


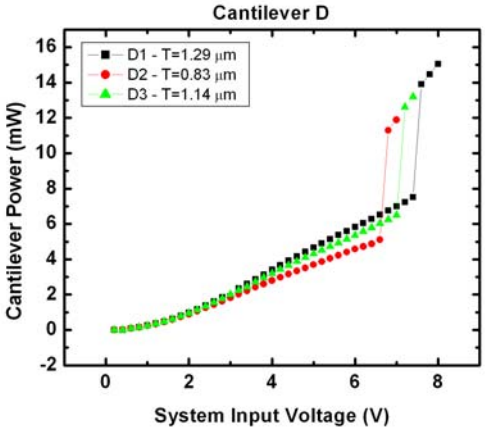


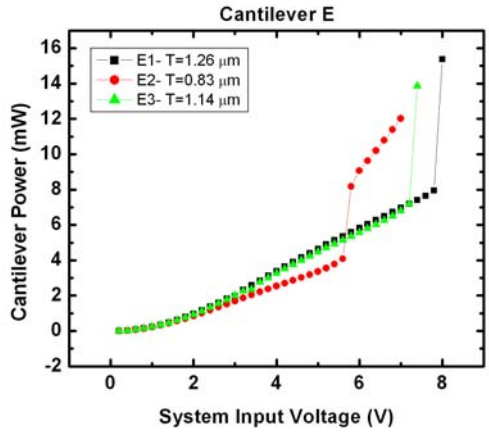
D2. Cantilever Power vs. System Input Voltage

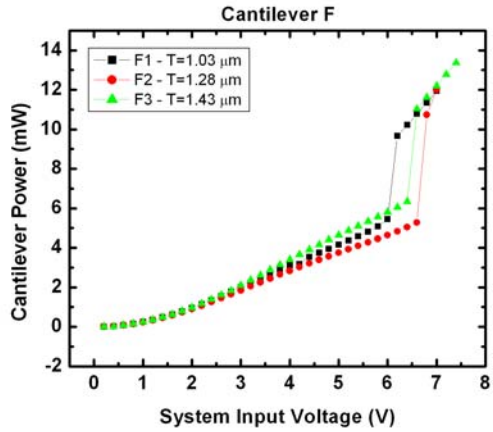




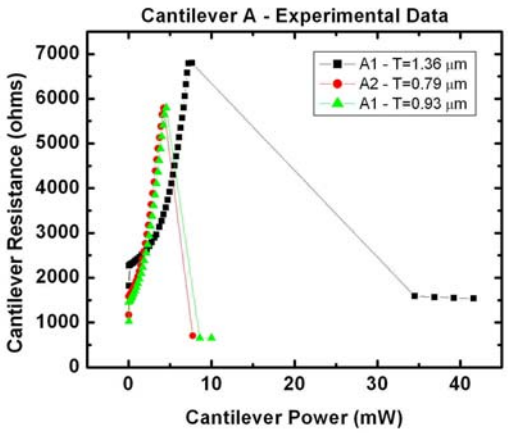


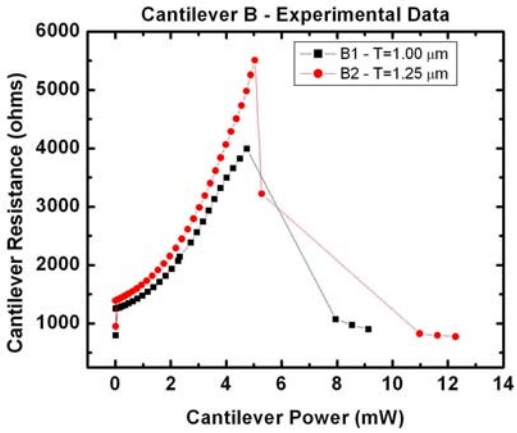


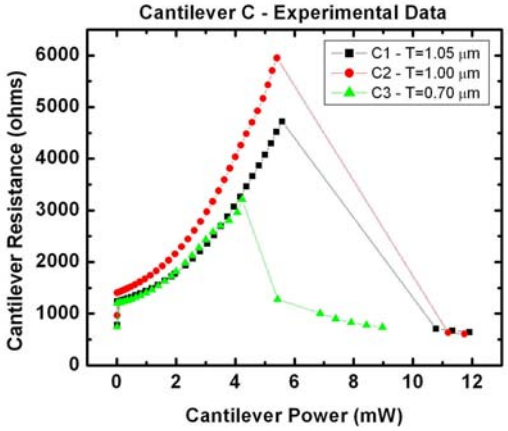


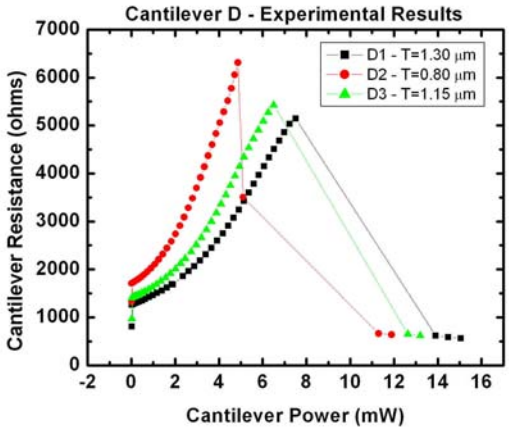


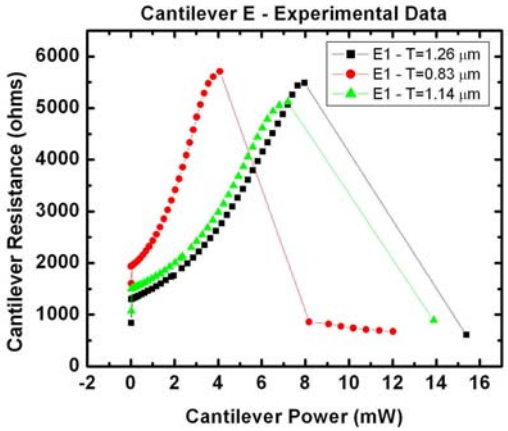
D3. Cantilever Resistance vs. Cantilever Power

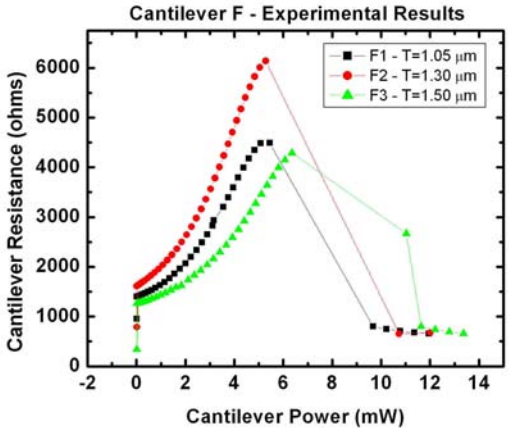








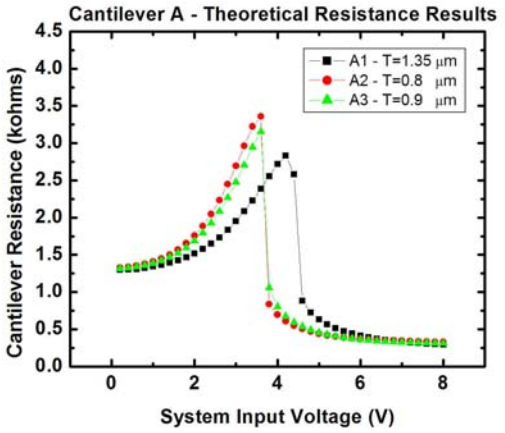


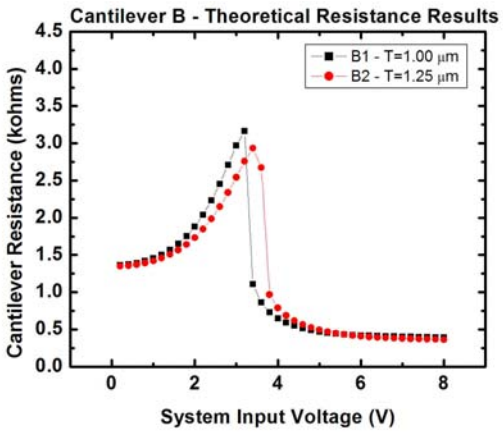


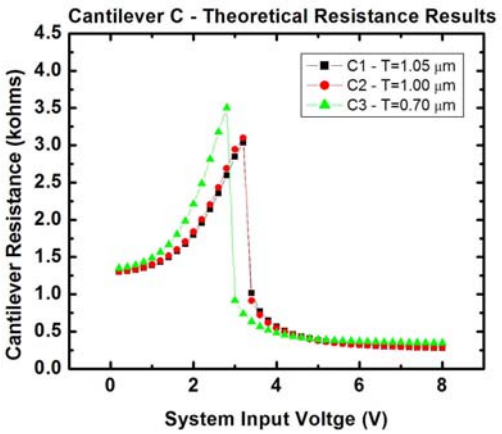
APPENDIX E

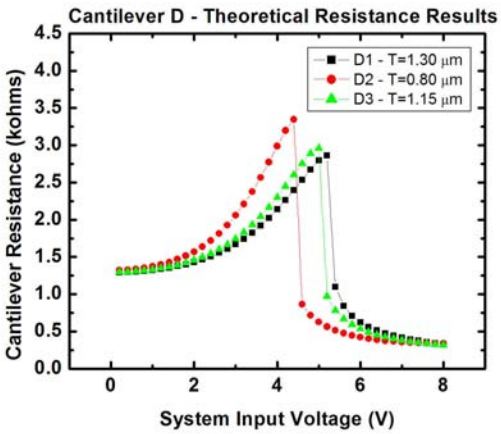
THEORETICAL RESULTS

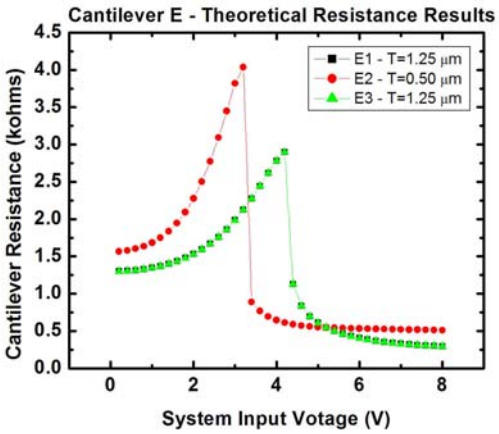
E1. Cantilever Resistance vs. System Input Voltage

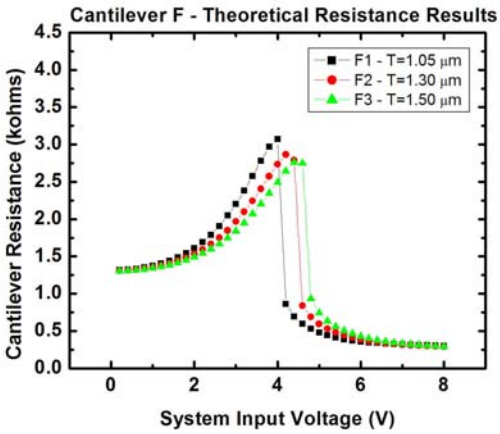




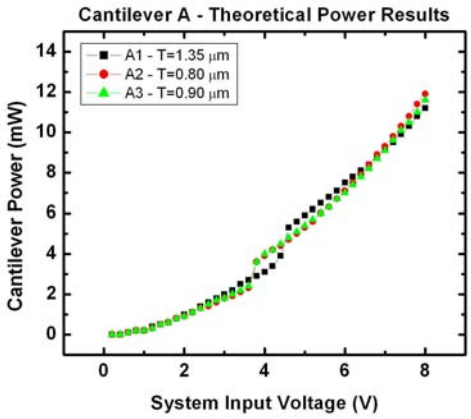


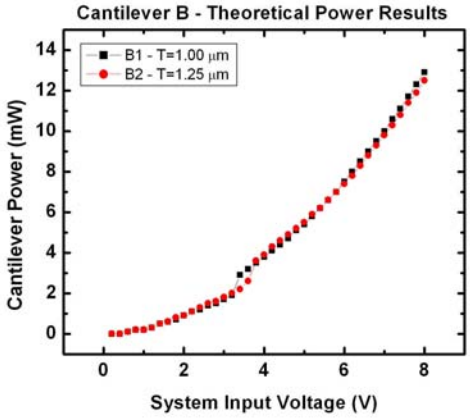


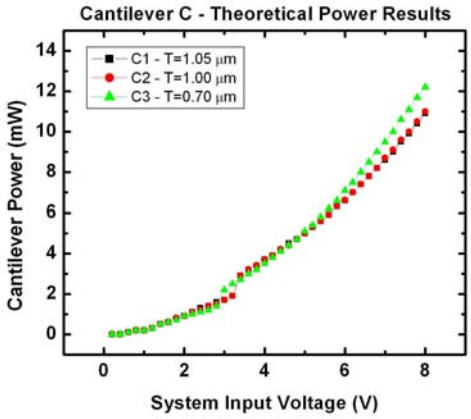


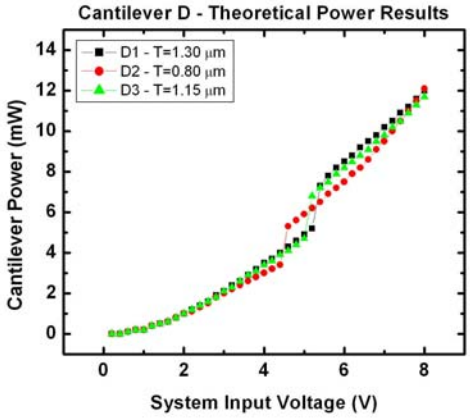


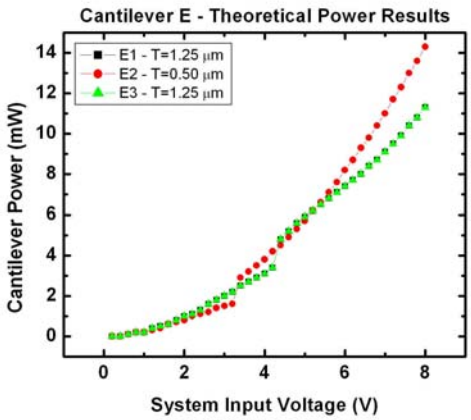
E2. Cantilever Power vs. System Input voltage

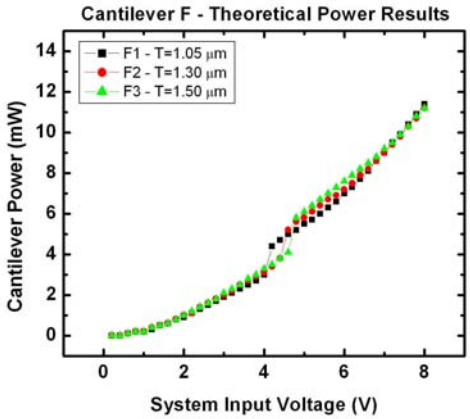




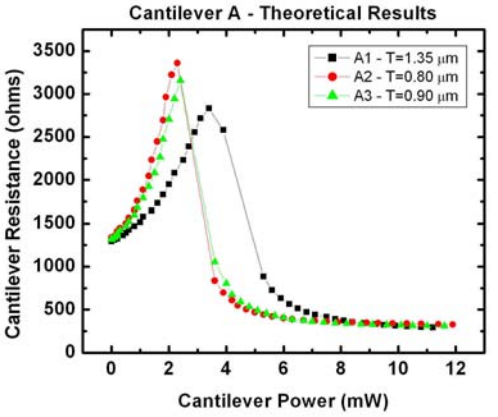


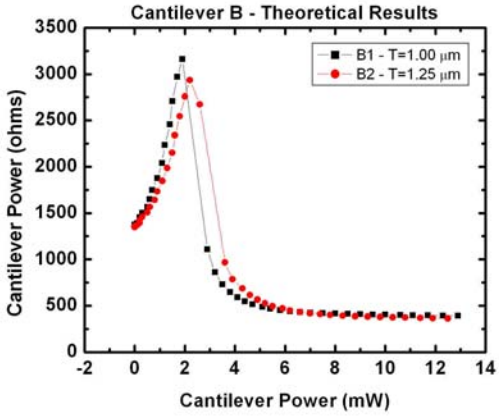


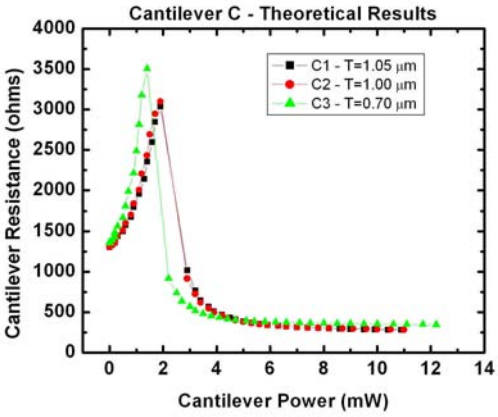


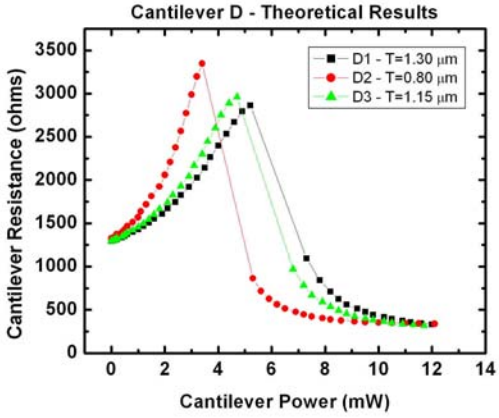


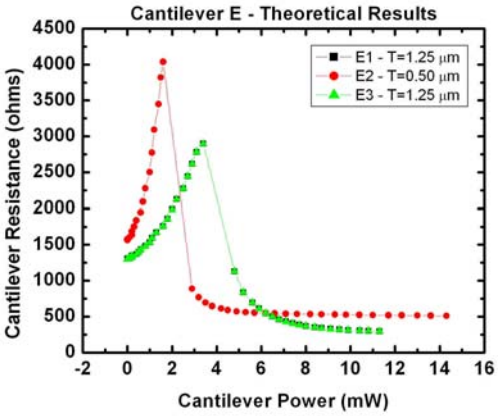
E3. Cantilever Resistance vs. Cantilever Power

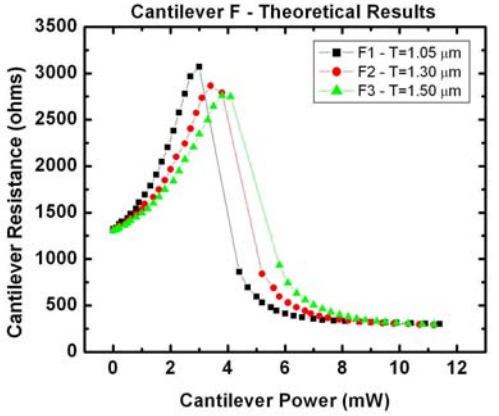












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